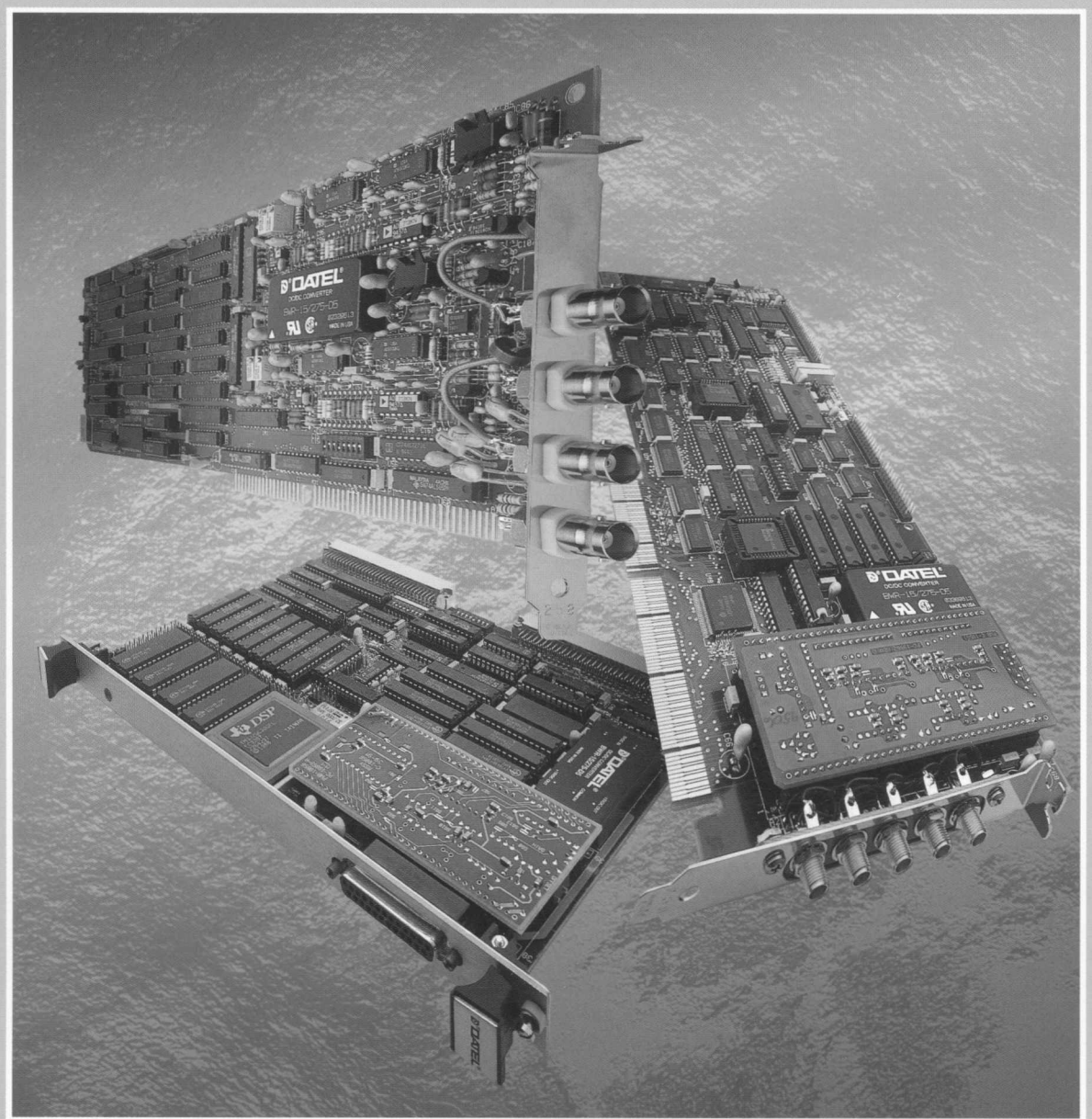
DATEL®

DATA ACQUISITION BOARDS



Analog I/O Boards for PCI, EISA, PC/ISA, VME and MULTIBUS I

DATEL Data Acquisition Boards

... for PCI, EISA, PC/ISA, VME and Multibus I

Speed by Architecture!

DATEL's data-acquisition and test-instrumentation boards offer the world's most advanced architectures for high-speed PC applications. Our boards feature wideband low-distortion inputs, simultaneous sampling on multiple channels (A/D per channel), on-board DSP's, and blazing speed. We pursue signal processing from a systems point of view. We understand the entire challenge of generating high-quality data and rapidly conveying it through hardware and software to its final destination. We design from the backplane up, combining clever architectural features such as fast streaming FIFO memory with quick low-level software to yield total system performance. Our goal is simple ... to deliver the world's best, high-speed signal conversion in a board-level format.

Quality by Design!

Modern board manufacturing is not trivial. Quality controls pervade our modern, mixed-technology, surface-mount/through-hole pc-board assembly facility. All of our boards are power-cycle burned in and fully tested with automatic test equipment. We also manufacture our own A/D and D/A converters. These high-performance microelectronic devices are built in the same MIL-STD-1772 certified facility supplying numerous military/aerospace programs. We control all aspects of product quality from vendor screening to outgoing inspection.

Build or Buy?

People sometimes question why they should buy our boards when they can simply build their own. The task is not simple. If you are a member of an extremely talented, multi-disciplined team that welcomes a challenge and has available time, your team may be able to duplicate our products. We highly recommend you take advantage of our many years experience with components, vendors, tricky CPU timing, different operating systems, mixed-technology assembly processes, etc. Use your valuable time to take advantage of our products ... not build them.

Convenience

DATEL has direct sales offices in the United States, Germany, France, England and Japan. We employ an extensive network of field sales representatives throughout the USA, Canada, Europe, the Far East and other areas around the world.

In the USA, dial 1-800-233-2765 to immediately receive literature, price and delivery information or applications assistance.

There are four different ways in which to purchase a DATEL Data Acquisition Board:

- VISA or Mastercard
- Bank check or money order
- C.O.D.
- Open an account with established credit





Availability

Most DATEL Data Acquisition Boards are in stock and can be shipped from the USA within 24 hours. For price and delivery information, USA customers should contact DATEL directly. Our international customers should contact their local DATEL office or sales representative. Evaluation boards are available on a consignment basis.

Applications Assistance

Our knowledgeable and patient staff of degreed applications and sales engineers will answer any technical questions and help you select the right board for your application. Customers in our subsidiary countries will find equally competent applications engineers in DATEL's direct sales offices.

Technical Literature

Each board is shipped with a high-quality, detailed user's manual that has been written for both the beginner and the expert.

We continually introduce new products and new analog front-end modules that fit into existing board families. Please contact us or one of our representatives for our latest product literature.

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Additional DATEL Literature

Individual Detailed Data Sheets

DATEL publishes a comprehensive data sheet for each of our products. Each data sheet includes detailed electrical performance specifications, applications information, mechanical dimensions, ordering information, etc. Please contact us for the data sheets you require.

Product Line Reference Catalogs

DATEL publishes a complete Product Line Catalog, which is essentially a compilation of data sheets plus additional technical information, for each of our major product lines:

- Data Acquisition and Conversion Components
- Analog I/O Boards for PCI, EISA, PC/AT, and VME buses
- Digital Panel Meters and Instruments
- DC/DC Converters

Contact us and you will immediately be sent the current edition of the volume(s) of your choice and be added to our mail list so you will receive new editions as soon as they are printed.

Application Notes

DATEL publishes a set of 9 application notes for data acquisition applications. We are currently preparing a similar set for DC/DC converter applications. Contact us if you would like to receive any or all of the application notes listed.

AN-1 High-Speed AD Converter Designs: Layout and Interfacing Pitfalls
AN-2 Picking the Right S/H Amp for Various Data Acquisition Needs
AN-3 Data Converters: Getting to Know Dynamic Specs
AN-4 Understanding Data Converters' Frequency Domain Specifications
AN-5 Subranging ADC's, Architectures, Specifications & Testing
AN-6 Seeing is Believing: A/D Converters Make the Difference in Imaging Applications
AN-7 Modifying Start Convert Pulses Using Commercially Available Devices
AN-8 Heat Sinks for DIP Data Converters
AN-9 Performance Considerations for High-End PC A/D Boards

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Internet Access

DATEL now has a short listing of our VME analog boards on the Internet. The listing is available from the following:

World Wide Web
http://www.cera.com/vmenet.htm

Via FTP
ftp.best.com /pub/cera as vmenet.txt
ftp.netcom.com /pub/ce/cera as vmenet.txt

Via E-Mail
Email cera@netcom.com
SEND VMENET in subject line

Our Internet E-mail address is **74557.2111@compuserve.com**

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- High-Speed/Resolution Data Conversion Components
- Modular DC/DC Power Converters
- Digital Panel Voltmeters and Instruments

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Analog Boards for PC/AT, PCI, and EISA Buses

25 years of responding to our customers' most demanding requirements has given DATEL a line of high-performance, analog-signal-processing boards for PC/AT (ISA), PCI, and EISA buses that is truly unique. Our analog I/O boards offer unmatched combinations of resolution, throughput, and dynamic range. Unique input configurations include 8 parallel channels of high-speed, 12-bit, simultaneous sampling. Clever architectures exploit on-board DSP coprocessors, FIFO's, and dual-port RAM's to permit high-speed (often beyond the bus limit), non-stop, continuous "streaming" of preprocessed data to memory or disk . . . with no lost samples. Other distinctive boards function as arbitrary waveform generators and programmable power supplies. Our products are different.

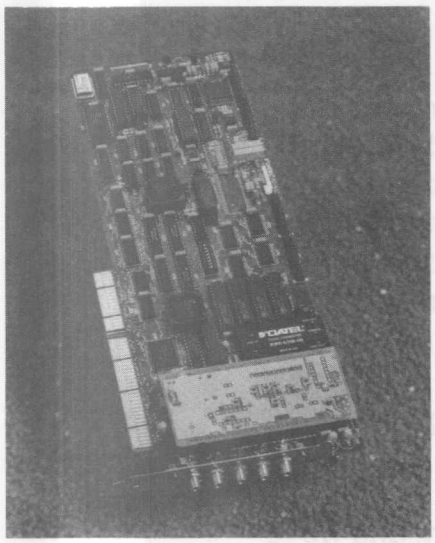
We're different. We offer patient, experienced application support, and we're more than happy to invest time discussing your individual requirement so that you may achieve an optimal solution.

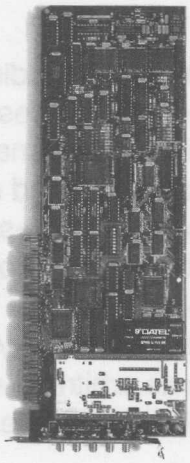
All of our board products are manufactured by DATEL, in the U.S.A., under the strictest quality controls. All boards are power-cycle burned in and are covered by a full one-year warranty.

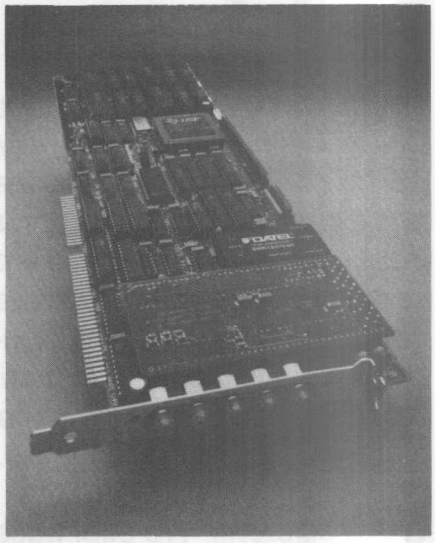
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New Products

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10MHz, 12-14 Bit Analog Input Boards for EISA Computers

PC-415 Family

- The ideal array-processor "front end"
- Up to 10MHz A/D sampling rates
- Choice of 12 or 14-bit A/D resolutions
- Wideband inputs with low harmonic distortion
- Quick, 32-bit, EISA block transfers
- 2/4/8-channel simultaneous sampling eliminates phase skew
- On-board A/D FIFO memory to 8k samples
- 32 megasamples or greater data streaming
- Pre/post-trigger, gap-free, ring buffering
- Great for DSP, FFT's, digital filtering, etc.
- Compatible with WINDOWS® and Pentium®

See page 1-23

PCI Compatible 10MHz, 12-14 Bit Analog Input Boards

PCI-416 Family

- The ideal array-processor "front end"
- Up to 10MHz A/D sampling rates
- Choice of 12 or 14-bit A/D resolutions
- Wideband inputs with low harmonic distortion
- Quick, 32-bit, PCI block transfers
- 2/4/8-channel simultaneous sampling eliminates phase skew
- On-board A/D FIFO memory to 8k samples
- 32 megasamples or greater data streaming
- Pre/post-trigger, gap-free, ring buffering
- Great for DSP, FFT's, digital filtering, etc.
- Pentium® compatible

See page 1-83

High-Performance Analog Input plus Advanced DSP Coprocessor

PC-430 Family

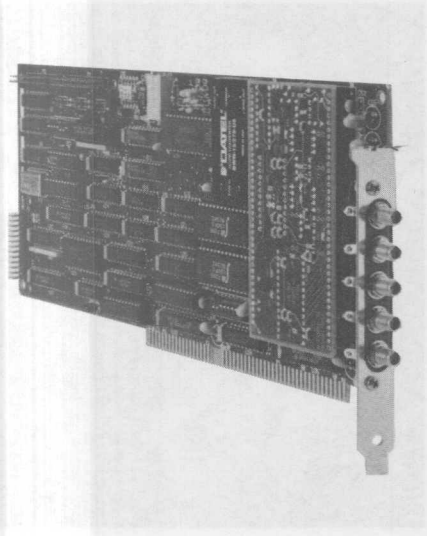
- Compatible with PC/AT, PS-30, and EISA computers
- Up to 10MHz A/D sampling rates
- Choice of 12 or 14-bit A/D resolutions
- 2/4/8-channel simultaneous sampling eliminates phase skew
- Local FIFO up to 4k A/D samples
- On-board TI 320C30 (32/40MHz) DSP
- Up to 4.5Mb dual-port RAM
- Two, 12-bit D/A channels (optional)
- Digital I/O (16 in, 16 out) (optional)
- RS-232 serial port, expansion ports, timers, internal or external trigger
- On-board DSP library - FFT's, windowing, filters, floating point, etc.
- Fast, simple, powerful Command Executive - no local programming
- WINDOWS® and Pentium® compatible, LabVIEW® available, model PC-430LV

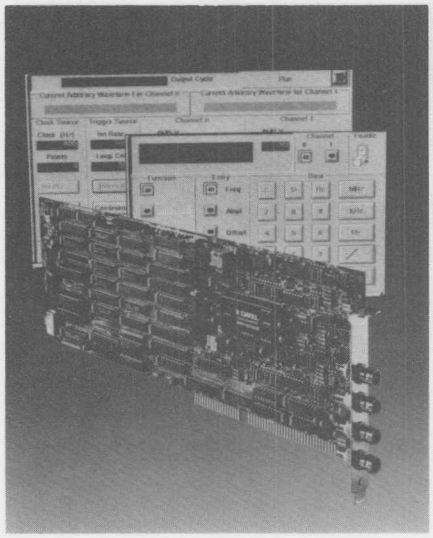
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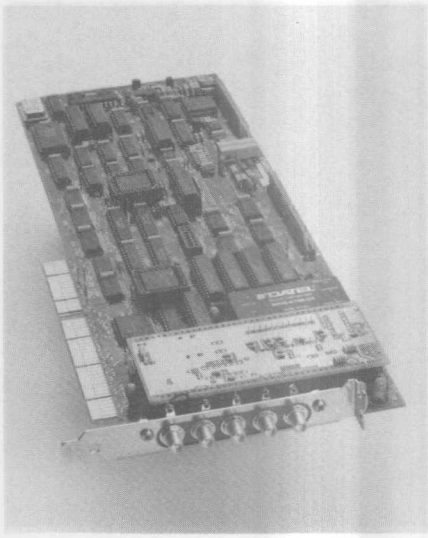
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New Products







Collect Millions of High-Speed, Analog Samples to Memory, Disk, or Parallel Port

PC-414 Family

- Compatible with PC/AT and EISA computers
- Up to 16 analog input channels
- Up to 10MHz A/D sampling rates
- Choice of 12 or 14-bit A/D resolutions
- 2/4/8-channel simultaneous sampling eliminates phase skew
- Programmable-threshold analog input trigger
- On-board FIFO up to 16k A/D samples for non-stop, gapless, data "streaming" to disk
- 10MHz DT Connect® parallel port avoids bus delays
- Very low harmonic distortion - ideal for DSP/FFT applications
- WINDOWS® and DOS software
- LabVIEW® drivers available, model PC-414LV

See page 1-15

High-Performance Low-Noise Arbitrary Waveform Generator

PC-420

- 2 simultaneous analog outputs with frequencies to 10MHz
- Sample update rates to 40MHz through two 12-bit D/A's
- High signal quality, –72dB THD
- On-board circular waveform memory, 32k samples per channel
- Store waveform samples on disk for playback
- High-resolution, frequency synthesized clock
- 8 software-selectable output filters per channel
- Software-programmable offset and gain
- "No programming" menued WINDOWS® software:
  - Signal waveform generator
  - Graphic waveform editor
- LabVIEW® drivers available, model PC-420LV

See page 1-35

8-Channel, 12-Bit, 250kHz Simultaneous Sampling Analog Input Board

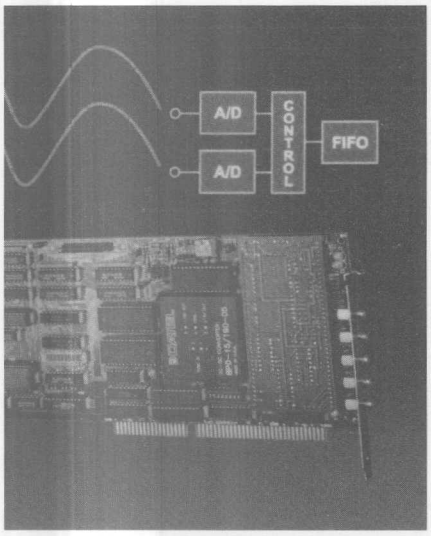
"J" Models of PC-414/415/430, PCI-416

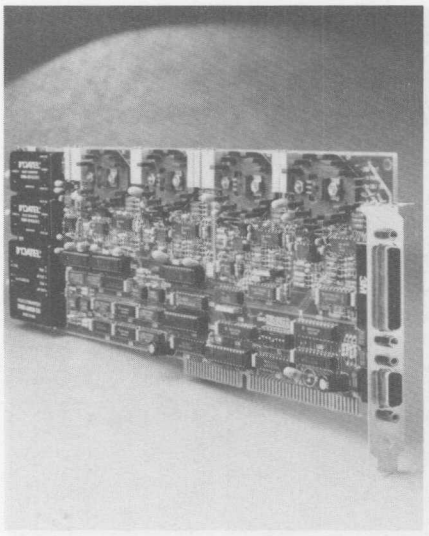
- 8 parallel analog input channels with concurrent sampling
- 8 independent, 12-bit, 250kHz A/D converters
- Eliminate phase skew on 8 parallel channels
- 100kHz input bandwidths
- –77dB total harmonic distortion
- Ideal for DSP/FFT applications
- On-board A/D FIFO memory up to 16k samples for non-stop data "streaming" to disk
- Throughput to FIFO:
  - 250kHz (single channel)
  - 2MHz (simultaneous channels)
- On-board TI 320C30 (32/40MHz) DSP (model PC-430J)
- LabVIEW® drivers available, "LV" series

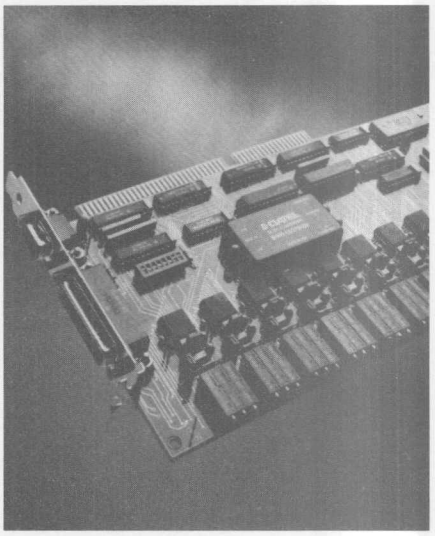
See pages 1-15, 23, 47, and 83

New Products

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2-Channel, 14-Bit, 1-2MHz Simultaneous Sampling Analog Input Board

"G" Models of PC-414/415/430, PCI-416

- Compatible with PC/AT, PC-30, EISA, and PCI computers
- 2 parallel analog input channels with simultaneous sampling functions
- 2 independent, 1MHz, 14-bit A/D converters (2MHz optional)
- 500kHz input bandwidths
- –80dB total harmonic distortion
- Ideal for DSP/FFT applications
- On-board A/D FIFO memory up to 16k samples for non-stop data "streaming" to disk
- Throughput to FIFO:
  1MHz (single channel)
  2MHz (simultaneous channels)
- On-board TI 320C30 (32/40MHz) DSP (model PC-430G)
- LabVIEW® drivers available, "LV" series

See pages 1-15, 23, 47, and 83

Quad-Output, Isolated Programmable Power Supply Board

PC-462

- 4 independently programmable, precise (12-bit), voltage outputs:
  0 to +6.15V @ 1 Amp
  0 to –6.15V @ 1 Amp
  0 to +20.5V @ 250mA
  0 to –20.5V @ 250mA
- All outputs fully isolated from PC/AT bus
- Remote sensing for each output
- Current limiting for each output
- 4 general-purpose analog inputs
- 2 isolated digital inputs
- 2 isolated relay-driver outputs
- "No programming" menued WINDOWS® software
- Free software driver library
- LabVIEW® VI available, model PC-462LV

See page 1-63

Generate 16 Fast Simultaneous Analog Outputs

PC-422

- 8 or 16 analog outputs from independent, 12-bit D/A's
- Individually selectable output ranges per channel: 0 to +5V/10V, ±5V, ±10V
- Double buffered digital input registers
- High-speed simultaneous block loading
- Simultaneous update for phase tracking and skew elimination
- On-board update clock or external event synchronization
- 3µsec settling, 330kHz update rate
- ±0.025% output linearity
- Trigger timer interrupt
- Discrete digital I/O (4 in, 4 out)
- Ideal for coherent waveform generation
- LabVIEW® drivers available, model PC-422LV

See page 1-43

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PC, EISA, and PCI bus Selection Tables

Combination Analog and Digital Input/Output

See page 1-9

Model	Input Channels①	Input Ranges②	A/D Resolution	A/D Conversion Rate	Output Channels	Digital I/O	Notes
PC-411A1	16SE/8D	0 to +5V or ±5V	12 bits	83kHz	—	8 in, 8 out	Expandable to 256SE/128D channels. Programmable gain amplifier (G = 1 to 100). On-board FIFO memory, DMA, and programmable interrupts for continuous "streaming" data acquisition. Simultaneous update (200kHz) for D/A's.
PC-411B1	16SE/8D	0 to +5V or ±5V	14 bits	59kHz	—	8 in, 8 out	
PC-411C1	16SE/8D	0 to +5V or ±5V	16 bits	27kHz	—	8 in, 8 out	
PC-412A1	16SE/8D	0 to +5V or ±5V	12 bits	83kHz	4, 12-bit D/A's	8 in, 8 out	
PC-412B1	16SE/8D	0 to +5V or ±5V	14 bits	59kHz	4, 12-bit D/A's	8 in, 8 out	
PC-412C1	16SE/8D	0 to +5V or ±5V	16 bits	27kHz	4, 12-bit D/A's	8 in, 8 out	
PC-440	32SE/16D	Slave A/D channel expander, cascadable up to 256SE/128D channels. *See page 1-61*					
PC-412SET	Setup, configuration, data save software - executables only. LabVIEW drivers available.						
PC-412SRC	Setup, configuration, data save software - source code and executables. LabVIEW drivers available.						
PC-490A/B	Screw termination - 9-pin (490A) or 25-pin (490B) or 37-pin (490C) or PC-440.						

①Input channel options are software-selectable. ②Input ranges are software-selectable.

High-Speed Analog Input Plus Memory for PC

See page 1-15

Model	Input Channels	Input Ranges	A/D Resolution	A/D Conversion Rate	Output Channels	Data Memory	Notes
PC-414A	4SE simul.	0 to +1V/10V, ±1V/10V①	12 bits	To 1.5MHz/chan.	1, 12-bit D/A	To 16ks FIFO	All models of the PC-414 have a programmable trigger/counter and a 10MHz parallel port. All have an on-board,12-bit D/A (200kHz update rate) and a programmable-threshold analog trigger.
PC-414B	4SE	0 to +10V, ±5V, ±10V	14 bits	To 500kHz	1, 12-bit D/A	To 16ks FIFO	
PC-414C	4SE	0 to +10V, ±5V, ±10V	12 bits	To 1.6MHz	1, 12-bit D/A	To 16ks FIFO	
PC-414D	1D	±5V	12 bits	To 5MHz	1, 12-bit D/A	To 16ks FIFO	
PC-414E	16SE/8D	50mV to 10V②	12 bits	To 2MHz	1, 12-bit D/A	To 16ks FIFO	
PC-414F	2SE simul.	0 to +10V, ±5V	12 bits	To 2MHz/chan.	1, 12-bit D/A	To 16ks FIFO	
PC-414G	2SE simul.	0 to +10V, ±5V	14 bits	To 1-2MHz/chan.	1,12-bit D/A	To 16ks FIFO	
PC-414H	1D	±5V	12 bits	To 10MHz	1, 12-bit D/A	To 16ks FIFO	
PC-414J	8SE simul.	0 to +2.5V, ±5V, ±10V	12 bits	To 250kHz/chan.	1, 12-bit D/A	To 16ks FIFO	
PC-414SET/WIN	Setup, configuration, data save software - executables only, MS-DOS or WINDOWS. LabVIEW drivers available.						
PC-414SRC/WINS	Setup, configuration, data save software - source code and executables, MS-DOS or WINDOWS.						

①Gains of 1 or 10 are user-selectable on 2 channels. ②Gain of 1 to 100 is resistor-programmable. See data sheet for full ordering information.

PC, EISA, and PCI bus Selection Tables

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High-Speed Analog Input Plus Memory for EISA

See page 1-23

Model	Input Channels	Input Ranges	A/D Resolution	A/D Conversion Rate	Output Channels	Data Memory	Notes
PC-415A	4SE simul.	0 to +1V/10V, ±1V/10V①	12 bits	To 1.5MHz/chan.	1, 12-bit D/A	To 8ks FIFO	The PC-415 employs a "banked" FIFO architecture to exploit 32-bit EISA block transfers. All have a programmable trigger/counter and a 10MHz parallel port. All have an on-board, 12-bit D/A (200kHz update rate) and a programmable-threshold analog trigger
PC-415B	4SE	0 to +10V, ±5V, ±10V	14 bits	To 500kHz	1, 12-bit D/A	To 8ks FIFO	
PC-415C	4SE	0 to +10V, ±5V, ±10V	12 bits	To 1.6MHz	1, 12-bit D/A	To 8ks FIFO	
PC-415D	1D	±5V	12 bits	To 5MHz	1, 12-bit D/A	To 8ks FIFO	
PC-415E	16SE/8D	50mV to 10V②	12 bits	To 2MHz	1, 12-bit D/A	To 8ks FIFO	
PC-415F	2SE simul.	0 to +10V, ±5V	12 bits	To 2MHz/chan.	1, 12-bit D/A	To 8ks FIFO	
PC-415G	2SE simul.	0 to +10V, ±5V	14 bits	To 1-2MHz/chan.	1,12-bit D/A	To 8ks FIFO	
PC-415H	1D	±5V	12 bits	To 10MHz	1, 12-bit D/A	To 8ks FIFO	
PC-415J	8SE simul.	0 to +2.5V, ±5V, ±10V	12 bits	To 250kHz/chan.	1, 12-bit D/A	To 8ks FIFO	
PC-415SET	Setup, configuration, data save software - executables only, MS-DOS.						
PC-415SRC	Setup, configuration, data save software - source code and executables, MS-DOS.						

①Gains of 1 or 10 are user-selectable on 2 channels. ②Gain of 1 to 100 is resistor-programmable. See data sheet for full ordering information.

Fast A/D-DSP Coprocessor and Software

See page 1-47

Model	Input Channels	Input Ranges	A/D Resolution	A/D Conversion Rate	Output Channels	Data Memory	Notes
PC-430A	4SE simul.	0 to +1V/10V, ±1V/10V①	12 bits	To 1.5MHz/chan.	2, 12-bit D/A's	To 4ks FIFO	All models of the PC-430 incorporate a 40MHz TI320C30 DSP CPU operating on a local, 32-bit data bus. All have installed 1/2Mb dual-port SRAM expandable to 4Mb, an on-board, programmable timer/counter, and offer multiple triggering schemes.
PC-430B	4SE	0 to +10V, ±5V, ±10V	14 bits	To 500kHz	2, 12-bit D/A's	To 4ks FIFO	
PC-430C	4SE	0 to +10V, ±5V, ±10V	12 bits	To 1.6MHz	2, 12-bit D/A's	To 4ks FIFO	
PC-430D	1D	±5V	12 bits	To 5MHz	2, 12-bit D/A's	To 4ks FIFO	
PC-430E	16SE/8D	50mV to 10V②	12 bits	To 2MHz	2, 12-bit D/A's	To 4ks FIFO	
PC-430F	2SE simul.	0 to +10V, ±5V	12 bits	To 2MHz/chan.	2, 12-bit D/A's	To 4ks FIFO	
PC-430G	2SE simul.	0 to +10V, ±5V	14 bits	To 1-2MHz/chan.	2, 12-bit D/A's	To 4ks FIFO	
PC-430H	1D	±5V	12 bits	To 10MHz	2, 12-bit D/A's	To 4ks FIFO	
PC-430J	8SE simul.	0 to +2.5V, ±5V, ±10V	12 bits	To 250kHz/chan.	2, 12-bit D/A's	To 4ks FIFO	
PC-430DAC	—	0 to +5V/10V, ±5V/10V③	—	100kHz④	2, 12-bit D/A's	—	PC-430 serial-port daughter modules, dual DAC or digital I/O. *See page 1-55.*
PC-430DIG	16TTL	Digital I/O	—	To 500kHz	16 TTL	—	
PC-430EXEC/WIN	"No programming" command scheduler, DSP library software (executables), MS-DOS or WINDOWS. LabVIEW drivers available.						
PC-430SRC/WINS	"No programming" command scheduler, DSP library software (full source code), MS-DOS or WINDOWS.						
PC-430HYPER	Hyperception integrated DSP display, save software, digital oscilloscope, spectrum analyzer.						
PC-430BUG	Assembly/C language debugger/monitor, single step, object file load/save software.						

①Gains of 1 or 10 are user-selectable on 2 channels. ②Gain of 1 to 100 is resistor-programmable.
③Output voltage ranges. ④D/A update rate See data sheet for full ordering information.

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PC, EISA, and PCI bus Selection Tables

High-Speed Analog Input Plus Memory for PCI

See page 1-83

Model	Input Channels	Input Ranges	A/D Resolution	A/D Conversion Rate	Output Channels	Data Memory	Notes
PCI-416A	4SE simul.	0 to +1V/10V, ±1V/10V①	12 bits	To 1.5MHz/chan.	1, 12-bit D/A	To 8ks FIFO	The PCI-416 employs a "banked" FIFO architecture to exploit 32- bit PCI block transfers. All have a programmable trigger/counter. All models have an on-board, 12-bit D/A (200kHz update rate) and a programmable-threshold analog trigger.
PCI-416B	4SE	0 to +10V, ±5V, ±10V	14 bits	To 500kHz	1, 12-bit D/A	To 8ks FIFO	
PCI-416C	4SE	0 to +10V, ±5V, ±10V	12 bits	To 1.6MHz	1, 12-bit D/A	To 8ks FIFO	
PCI-416D	1D	±5V	12 bits	To 5MHz	1, 12-bit D/A	To 8ks FIFO	
PCI-416E	16SE/8D	50mV to 10V②	12 bits	To 2MHz	1, 12-bit D/A	To 8ks FIFO	
PCI-416F	2SE simul.	0 to +10V, ±5V	12 bits	To 2MHz/chan.	1, 12-bit D/A	To 8ks FIFO	
PCI-416G	2SE simul.	0 to +10V, ±5V	14 bits	To 1-2MHz/chan.	1,12-bit D/A	To 8ks FIFO	
PCI-416H	1D	±5V	12 bits	To 10MHz	1, 12-bit D/A	To 8ks FIFO	
PCI-416J	8SE simul.	0 to +2.5V, ±5V ±10V	12 bits	To 250kHz/chan.	1, 12-bit D/A	To 8ks FIFO	
PCI-416WIN	Setup, configuration, data save software - executables only, WINDOWS.						
PCI-416WINS	Setup, configuration, data save software - source code and executables, WINDOWS.						

①Gains of 1 or 10 are user-selectable on 2 channels. ②Gain of 1 to 100 is resistor-programmable. Contact DATEL for new analog modules. See data sheet for full ordering information.

Fast, Simultaneous Analog Output

See page 1-43

Model	Output Channels	Output Ranges	D/A Resolution	D/A Update Rate	Digital I/O	Trigger Timer Interrupt	Notes
PC-422A	8 simul.	0 to +5V, +10V, ±2.5V, ±5V, ±10V	12 bits	330kHz	4 in, 4 out	500ns to 537 sec.	Arbitrary waveform/function generators. Simultaneous update. Output ranges selectable per channel.
PC-422B	16 simul.	0 to +5V, +10V, ±2.5V, ±5V, ±10V	12 bits	330kHz	4 in, 4 out	500ns to 537 sec.	
PC-422SET	Setup, data load, file playback software - executables only						
PC-422SRC	Setup, data load, file playback software - source code						

PC, EISA, and PCI bus Selection Tables

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Test Instrumentation

Model	Description	Analog I/O Channels	Notes
PC-462	Programmable power supply board	4 isolated outputs: 0 to +6.15V/-6.15V @ 1A 0 to+20.5V/-20.5V @250mA. 4 isolated inputs (±5V)	4 isolated digital channels (2 in, 2 out) 12-bit A/D-D/A conversion, remote load sense. *See page 1-63*
PC-462SET	Configuration, display/load software for WINDOWS (executables), LabVIEW software available.		
PC-462SRC	Configuration, display/load software for WINDOWS (source code)		
PC-420	Arbitrary waveform generator	2 simultaneous outputs: update rates to 40MHz, 12-bit D/A's, programmable offset/attenuation	64k waveform RAM per channel, external trigger, 8 selectable filters. *See page 1-35*
PC-420SET	Configuration, waveform load/edit software for WINDOWS (executables), LabVIEW software available		
PC-420SRC	Configuration, waveform load/edit software for WINDOWS (source code)		
PC-EL Series	Voltage-controlled Electonic Loads		1 to 25A (2V to 500V), 400W. *See page 1-75*
PC-465	Electronic Load Controller Board		Fully programmable, virtual instrument. *See page 1-71*
PC-465WIN	Windows setup/configuration program		
PC-465WINS	Source code for PC-465WIN		
PC-467	Power Supply Measurement Board		Measures input/output power supply parameters. *See page 1-79*
PC-467WIN	Windows setup/configuration program		
PC-467WINS	Source code for PC-467WIN		
PC-467PWRSYS	Complete power supply test system software		

LabVIEW® Bridge Software Virtual Instrument Library

Starting on page 1-89

Model	Calibration Config./Setup	Self-Test	Front Panel	Get Data	Notes	Source Code
PC-412LV,LVS	✓	✓	✓	Optional DDE	Includes demo	PC-412LVS
PC-414LV,LVS	✓	✓	✓	Optional DDE	Includes demo	PC-414LVS
PC-420LV,LVS	✓	✓	✓	Optional DDE	Inlcudes demo	PC-420LVS
PC-422LV,LVS	✓	✓	✓	Optional DDE	Includes demo	PC-422LVS
PC-430LV,LVS	✓	✓	✓	Optional DDE	Includes demo	PC-430LVS
PC-462LV,LVS	✓	✓	✓	Optional DDE	Includes demo	PC-462LVS

"LV" models include all executable code and icon files.
"LVS" models consist of all "LV" files plus all source code.
All systems require LabVIEW on the host.

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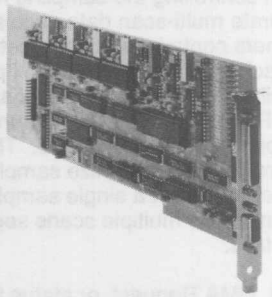
PC-411, PC-412

16-Channel, Analog I/O Boards with FIFO for IBM-PC® Computers

FEATURES

- **16SE or 8D analog input channels, expandable to 256**
- **4 Analog output channels optional (PC-412) with simultaneous update**
- **Choice of 12, 14, or 16-bit A/D resolution**
- **On-board programmable trigger clock**
- **Discrete digital I/O (8 input, 8 output)**
- **FIFO memory, DMA, and programmable interrupts for continuous, non-stop, "streaming" data acquisition**
- **Programmable gain amplifier**
- **Signal conditioning per channel**

Now with LabVIEW® VI's



GENERAL DESCRIPTION

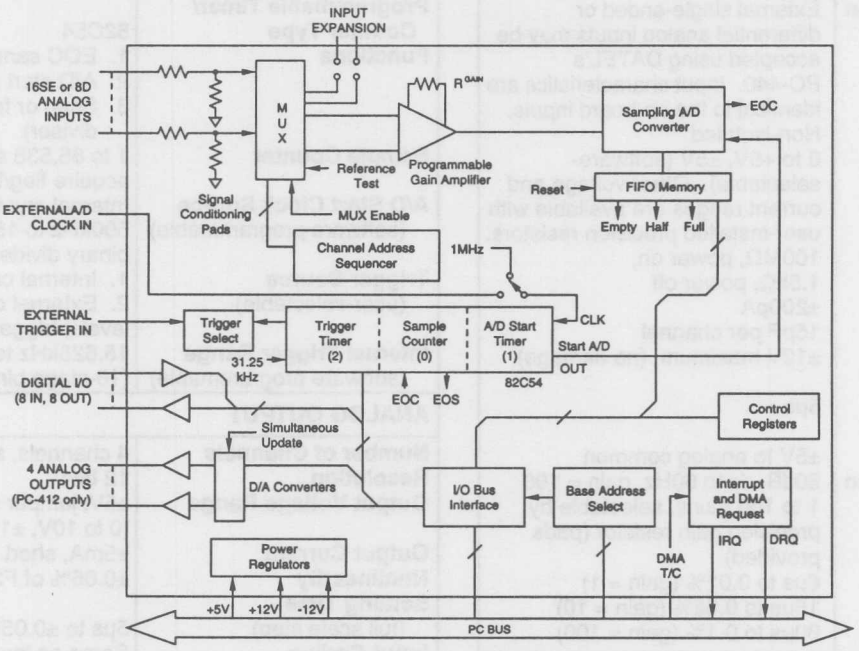
Offering non-stop continuous collection of up to 16 analog input signals in real time, the PC-411 is an analog input board for IBM-PC, PC/XT, PC/AT, and compatible computers. The PC-411 accepts 16 single-ended or 8 differential input signals, digitizes them up to 12, 14, or 16-bit resolution and places them on the computer bus under software control. Data may then be stored in PC memory, saved on disk, or displayed on the screen or printer.

Model PC-412 is a combination analog input and output board using the same input section as the PC-411. The PC-412 adds four optional analog output channels to be used for chart recorders, actuator controllers, or other output devices. Both the PC-411 and PC-412 accept external analog input expansion channels. On both the PC-411 and PC-412, sixteen discrete digital I/O lines are configured as 8 inputs and 8 outputs for external logic devices. The digital outputs can control the channel addressing of an expansion input multiplexer.

The differential analog inputs offer rejection of common mode noise while the on-board Programmable gain amplifier (PGA) offers higher gains (up to times 100) for low-level sensors. On-board circuit pads on each channel may be configured for other input voltage or current ranges or input signal conditioning.

Analog-to-digital converter (A/D) data passes to an on-board First-In, First-Out (FIFO) data memory. FIFO data is then transferred to the host computer bus interface under software control. Besides temporarily storing a block of samples, the FIFO acts to decouple the precise timing of the A/D section from the block-oriented data transfer burst on the bus.

Unlike many other analog input boards for the PC, the PC-411/412 can continuously collect analog data with non-stop converter triggering while data is simultaneously read by the PC from the FIFO. This allows the collection of "seamless" signals of millions of samples or greater. Another advantage of the FIFO is high-speed disk recording of analog data with no loss of samples during disk writes.



PC-411/412 Block Diagram

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MS-DOS is a trademark of Microsoft Corporation

GENERAL DESCRIPTION CONT.

Expansion up to 256SE/128D total channels is offered on DATEL's PC-440 MUX board in increments of 32SE/16D channels.

The timing section controlling the sampling A/D converter is designed for accurate multi-scan data acquisition. Software programmable timers control the interval between each conversion and each multichannel scan. A programmable sample counter will allow sample blocks of specified length independent of FIFO length. The timer/counter section uses an internal clock or an external timebase. The external trigger may be used to precisely synchronize sampling with external events. The trigger may start a single sample, a single multi-channel scan, or "N" multiple scans separated by programmable delays.

Either an interrupt, DMA Request, or status flag indicates when FIFO data is ready. Normally, a FIFO interrupt from the PC-411/412 triggers the PC to burst a fixed-length block of samples to host PC memory. This offers very high overall system speed by not tying up the bus and allows the PC to continue with graphics, math, or disk activities.

The PC-412 analog output channels include a simultaneous update option where all channels drive their outputs to new values at the same time from a software trigger. Applications for this include phase-synchronous system simulation, process control, and coherent field waveform generation.

Most options are software configured, reducing the number of jumpers required. Window-driven software is available on MS-DOS disks to configure the board and save data. A comprehensive user's manual is also included.

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted)

ANALOG INPUTS	
Number of Channels (software-selectable)	16 single-ended or 8 differential channels
Input Channel Expansion	External single-ended or differential analog inputs may be accepted using DATEL's PC-440. Input characteristics are identical to the on-board inputs.
Input Configuration	Non-isolated
Full Scale Input Ranges (gain = 1)	0 to +5V, ±5V (software-selectable). Other voltage and current ranges are available with user-installed precision resistors.
Input Impedance	100MΩ, power on, 1.5kΩ, power off
Input Bias Current	±200pA
Input Capacitance	15pF per channel
Input Overvoltage	±12V maximum (no damage)
Overvoltage Recovery Time	5µs
Common Mode Voltage Range	±5V to analog common
Common Mode Rejection	80dB, dc to 60Hz, gain = 100
Programmable Gain Amplifier	1 to 100 gains, selectable by precision gain resistor (pads provided)
PGA Settling Delay	6µs to 0.01% (gain = 1) 15µs to 0.02% (gain = 10) 80µs to 0.1% (gain = 100)

A/D CONVERTER	
Resolution	12 bits (PC-411/412A) 14 bits (PC-411/412B) 16 bits (PC-411/412C)
A/D Conversion Period	7µs (PC-411/412A) 14µs (PC-411/412B) 32µs (PC-411/412C)
Aperture Time	25ns
Acquisition Time	3µs
Output Coding	Positive-true, left-justified, straight binary (unipolar) or offset binary (bipolar)
Trigger Sources (software-selectable)	1. Local Pacer sample clock 2. External digital sample clock
Addressing Modes	1. Single channel 2. Sequential with autosequenced addressing 3. Random addressing by host software

INPUT SYSTEM PERFORMANCE	
Integral Nonlinearity	±0.05% of FSR (PC-411/412A) ±0.015% of FSR (PC-411/412B) ±0.005% of FSR (PC-411/412C)
Differential Nonlinearity	±0.5 LSB (±1 LSB 411/412B,C)
Full Scale or Zero/Offset	±0.1 LSB per °C (PC-411/412A)
Temperature Coefficient	±0.3 LSB per °C (PC-411/412B,C)
Monotonicity	No missing codes
Power Supply Rejection	±0.01% of PC bus ±12V
Total Scan Throughput (sample-to-sample with sequential addressing)	17µs (PC-411/412A) 23µs (PC-411/412B) 42µs (PC-411/412C) (see Notes)
Total Throughput (no channel advance)	12µs (PC-411/412A) 17µs (PC-411/412B) 37µs (PC-411/412C)

A/D MEMORY	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	512 A/D samples

TRIGGER CONTROL	
Programmable Timer/ Counter Type	82C54
Functions	1. EOC sample count 2. A/D start rate (16-bit divisor) 3. Scan or frame rate (16-bit divisor)
Sample Counter	1 to 65,536 samples. Drives the acquire flag/interrupt.
A/D Start Clock Source (software programmable)	Internal crystal clock. Range 500kHz to 15.26Hz (16-stage binary divider or BCD).
Trigger Source (user-selectable)	1. Internal crystal clock 2. External digital input. TTL levels, triggers on falling edge.
Internal Trigger Range (software programmable)	15.625kHz to 2.097 seconds (16-stage binary divider or BCD)

ANALOG OUTPUT	
Number of Channels	4 channels, single-ended
Resolution	12 bits
Output Voltage Range	±5V, jumper selectable per chan. (0 to 10V, ±10V special order)
Output Current	±5mA, short circuit protected.
Nonlinearity	±0.05% of FSR
Settling Time (full scale step)	5µs to ±0.05% of FSR
Input Coding	Same as input section
Temperature Coefficients	Same as input section

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PC BUS INTERFACE	
Architecture	Decodes 16 byte-wide I/O registers using address lines A9-A0. Highest base address is 3F0h.
Data Bus Width	8 bits
PC Bus Interrupt (software maskable)	1 line, software selectable IRQ 3, 5, 7.
Bus Interrupt Sources	Scan acquire flag (sample count). FIFO full, half full or not empty or DMA T/C.
Bus Data Transfer Rate	1 Megabyte/second or greater, dependent on host PC
Direct Memory Access	1 line, software-selectable, DRQ1 or DRQ3 from FIFO HF, FF, EF, or ACQ
PARALLEL PORT	
Parallel Outport	8 lines, TTL levels, 24mA out
Parallel Inport	8 lines, TTL levels, 2mA in plus pullup resistor to +5V
CONNECTORS	
Analog Inputs, P1	25-pin female DB-25S connector on rear mounting bracket for analog inputs and trigger
Analog Outputs, P2 (PC-412 only)	9-pin female DB-9S connector on rear mounting bracket
Parallel Port	Internal header connector, 0.025 inch pins on 0.100 inch spacing, suitable for flat cable
PC Bus Connector, P3	Edgeboard connector
MISCELLANEOUS	
Power Required (PC-411)	+5V, ±5% at 1A max. and ±12V, ±5% at 100mA max. all supplied from the bus
(PC-412)	+5V: 2A max. ±12V: 250mA max.
Operating Temperature Range	0 to +60°C Forced cooling is recommended.
Storage Temperature Range	-20 to +80°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet
Outline Dimensions	4.2" H x 13.31" L x 0.625" D (11,43 x 33,81 x 1,59 cm) compatible to PCbus
Weight	10 ounces (290 grams)
Analog Section Adjustments	Inputs: offset and gain Outputs: offset and gain per channel

NOTES/DEFINITIONS

Input Settling Delays:
The PC-411/412 will run faster in single channel operation than multichannel after the input is settled on the first channel. Total sample-to-sample throughput time must include input multiplexer settling time after changing the channel address, PGA settling time (depending on the gain), sampling A/D converter acquisition time, and A/D conversion time.

The PC-411/412 sampling rate will not be delayed by FIFO-to-PC data transfers if the FIFO is not full.

Sampling Rate per Channel
The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling delays. For example, if four channels were scanned, the maximum sample rate on any one channel of the PC-411/412A would be 17 microseconds times 4 channels, equalling 68 microseconds (14.7kHz per channel). Observe Nyquist sample rate rules for inputs with unknown spectral content.

To avoid overload recovery delays, do not let the analog input exceed the input voltage range.

Highest total system speeds will be achieved if the FIFO is block transferred using DMA or the REP INS instruction in a loop with the CX register controlling the count of samples transferred.

Scan:
A scan would consist of a group of channels sampled together with equal delays between each A/D sample, set by the A/D start clock. A scan is 16S or 8D channels or less. A scan uses sequential channel addressing.

Frame:
Frames are one or more channels sampled together at each trigger with equal delays between each A/D sample, set by the A/D start clock. Each frame is started by one trigger. Either single channel or autosequential scan addressing may be used. A frame may consist of several contiguous scans with wrap around addressing. Frames are stopped when the counter 0 Acquire bit is reset to zero.

PROGRAMMING

(Refer to the PC-411/412 user manual for detailed programming information.)

The BASE address may be selected anywhere up to 3F0h on 16-byte boundaries. At power up or PCbus reset, all registers contain zeroes except the FIFO HF and FF bits. When setting one bit in a write only register, remember to select all other bits according to the desired code. A shadow register should be considered to store the last value written. The registers may be programmed in any sequence as long as the command register is last. "x" bits are don't care or not used.

I/O REGISTER MAPPING

I/O Address (Hex)	Direction	Description
BASE + 0	Write	Command Register
BASE + 0	Read	Status Register
BASE + 1	Write	Channel Address Register
BASE + 1	Read	FIFO A/D Data Register
BASE + 2	Write	Interrupt/DMA Register
BASE + 2	Read	FIFO Reset Register
BASE + 3	Write	Digital Output Port
BASE + 3	Read	Digital Input Port
BASE + 4	Read/Write	Counter #0 (82C54)
BASE + 5	Read/Write	Counter #1 (82C54)
BASE + 6	Read/Write	Counter #2 (82C54)
BASE + 7	Read/Write	Control Word (82C54)
BASE + 8	Write	DAC 0 low byte
BASE + 9	Write	DAC 0 high byte
BASE + 10	Write	DAC 1 low byte
BASE + 11	Write	DAC 1 high byte
BASE + 12	Write	DAC 2 low byte
BASE + 13	Write	DAC 2 high byte
BASE + 14	Write	DAC 3 low byte
BASE + 15	Write	DAC 3 high byte

COMMAND REGISTER (Write BASE + 0)

7	6	5	4	3	2	1	0
A/D Calib	Chan Expnd	Read A/D Ref	SE/ Diff	Unipolar or Bipolar	Auto Incr	A/D Conv Enbl	Trig Int/ Ext

Trigger Select [Bit 0]
0 = Internal trigger from 82C54 timer 2.
1 = External digital trigger

A/D Converter Enable [Bit 1]
0 = Disable A/D conversion
1 = Enable A/D conversion

Both command bit 1 and the counter 0 ACQuire gate must be set to enable A/D conversions.

Channel Address Autoincrement [Bit 2]
0 = Single channel (no increment)
1 = Sequence channel address after A/D conversion.

In autoincrement, the channel address advances on the A/D EOC rising edge. For continuous scanning, the address wraps around to channel 0 after reaching channel 15, modulo 16. Eight-channel boards wrap after channel 7. Allow adequate settling time before starting the next A/D conversion. In single-channel mode, the A/D may be triggered as fast as the EOC appears.

Unipolar/Bipolar [Bit 3]
0 = A/D input range is 0-5V.
1 = A/D input range is ±5V.

Single-ended/ Differential [Bit 4]
0 = Input configuration is single-ended, 16 channels.
1 = Input configuration is differential, 8 channels.

Read A/D Reference [Bit 5]
0 = Normal input sampling
1 = Select reference input

This bit selects a +4.5V reference channel on the A/D converter to verify A/D operation. It is not used for calibration.

Input Channel Expansion [Bit 6]
0 = Enable local channels, disable expansion inputs.
1 = Disable local channels, enable expansion inputs.

Bit 6 switches a downstream multiplexer between the local channel multiplexer and the differential expansion input channel. If an external user-supplied multiplexer is used for expansion channels, control external channel addressing using the parallel digital outputs.

Calibrate A/D Converter [Bit 7]
0 = Normal operation
1 = Start calibration cycle

Writing a one to this bit then resetting it back to zero begins an A/D linearization sequence. This takes approximately 20 milliseconds until EOC. Perform this operation once after power up. During calibration, the A/D converter makes internal corrections. Periodic calibration is optional in stable temperature environments but is suggested frequently with significant temperature changes.

STATUS REGISTER (Read BASE + 0)

7	6	5	4	3	2	1	0
End of Conv	FIFO Full*	FIFO Half Full*	FIFO Empty*	Acquire Status	Auto Incr Enbl	A/D Conv Enbl	Trig Int/ Ext

Bits 0, 1, and 2 echo the corresponding command register bits and verify proper register loading.

Acquisition Status [Bit 3]
0 = A/D scan not in progress or scan is done. (Counter 0 EOC sample count was reached). The A/D is disabled.
1 = A/D scan in progress.(Counter 0 EOC sample count was not reached).

The ACQuire bit resets to zero after a fixed number of samples (up to 65,536) have been transferred to the FIFO. The sample count is set by Counter 0. The A/D start clock is inhibited when ACQ is 0. A special mode allows continuous non-stop A/D triggering for frames larger than 65K by counting FIFO transfers in software. ACQ is not valid until the FIFO starts filling.

FIFO Memory Status Flags
Bit 4: 0 = FIFO is empty, 1 = FIFO is not empty.
Bit 5: 0 = FIFO is half full or greater. 1 = FIFO is less than half full.
Bit 6: 0 = FIFO is full 1 = FIFO is not full.

*Note the negative true coding on these bits.

End of A/D Conversion Status (EOC) [Bit 7]
See User Manual.

Note that all data transfer is through the FIFO. Use the FIFO signals instead of EOC to tell when data is ready. EOC clocks A/D data into the FIFO.

INPUT CHANNEL ADDRESS REGISTER (Write BASE + 1)

7 - 4	3 2 1 0
Not Used	Start Channel Address

Start Channel Address [Bits 3-0]

In single-channel mode, these bits select the address of the next input channel for A/D conversion.

In autoincrement mode, bits 3-0 are the starting channel address. After each A/D conversion, the EOC automatically sequences the address. The address wraps around to channel 0 after reaching channel 15 in single-ended mode or channel 7 in differential mode. If an exact multiple of 8D or 16S channels is triggered, and the user's program counts samples, the channel address will not need reloading. The user must count samples read from the FIFO to determine the current channel address or must periodically reload the starting address.

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FIFO A/D DATA REGISTER (Read BASE + 1)

First Read (most significant byte):

7	6	5	4	3	2	1	0
AD 9	AD 10	AD 11	AD 12	AD 13	AD 14	AD 15	AD 16
			12-bit LSB		14-bit LSB		16-bit LSB

Second Read:

7	6	5	4	3	2	1	0
AD 1	AD 2	AD 3	AD 4	AD 5	AD 6	AD 7	AD 8
MSB ALL							

A/D data is presented in two sequential reads at the same output port location. The least significant byte is read first. The data is left justified and unused least significant bits are zeroes. Note that A/D data assigns the MSB as A/D bit 1. For bipolar inputs, the MSB indicates polarity (0 = negative, 1 = positive).

INTERRUPT CONTROL REGISTER (Write BASE + 2)

7	6	5 4	3 2	1 0
Simultaneous DAC Update	Not Used	DMA Level 1 0	Interrupt Level 1 0	Int/DMA Source 1 0

Hardware flags in the PC-411/412 may cause either an interrupt or a DMA request. If both an interrupt and DMA are enabled, an interrupt will be generated by the PCbus DMA Terminal Count signal only.

Interrupt or DMA Source

Bits 1 0
- 0 0 = Interrupt request at FIFO full flag.
- 0 1 = Interrupt request at FIFO half full flag.
- 1 0 = Interrupt request at Data Acquire flag. Counter 0 EOC sample count reached.
- 1 1 = Interrupt or DMA request at FIFO not empty flag. Each sample will cause a DMA request if enabled.

This last mode will allow single A/D samples to transfer on each DMA request. Load the DMA controller count register with the number of samples to be transferred. When the Terminal Count is reached, (with optional interrupt) reprogram the DMA controller then process the previous DMA buffer.

Interrupt Level

Bits 3 2
- 0 0 = Interrupt disable
- 0 1 = Interrupt request on the IRQ 3 line
- 1 0 = Interrupt request on the IRQ 5 line
- 1 1 = Interrupt request on the IRQ 7 line

DMA Level Select

Bits 5 4
- 0 0 = DMA disable
- 0 1 = DMA request on DRQ 1 line
- 1 0 = DMA request on DRQ 3 line
- 1 1 = Spare

Only block mode DMA transfers are available (no single samples).

Simultaneous DAC Update [Bit 7]
- 0 = Writing to a DAC high byte register will update that channel.
- 1 = All DAC's will simultaneously update when bit 7 is toggled to zero then back to one.

If bit 7 = 1, writing to a DAC will not update that channel but data will be stored for later simultaneous update.

FIFO MEMORY RESET REGISTER (Read BASE + 2)

7 - 0
x - x

Reading this register clears the FIFO and sets the empty flag true. All previous FIFO data is lost. If A/D conversion is still running, the FIFO will not be empty when the next A/D EOC occurs.

DIGITAL OUTPORT REGISTER (Write BASE + 3)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0

Discrete digital outputs are loaded in these bits.

DIGITAL INPORT REGISTER (Read BASE + 3)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0

Discrete digital inputs are read in these bits.

82C54 PROGRAMMABLE INTERVAL TIMER

Counter Register
- (Read/Write BASE + 4 - Counter #0)
- (Read/Write BASE + 5 - Counter #1)
- (Read/Write BASE + 6 - Counter #2)

7	6	5	4	3	2	1	0
C07	C06	C05	C04	C03	C02	C01	C00

Counter 0 counts up to 65,536 A/D samples (load one less than the desired number of samples). Counter 0 inhibits A/D conversions when the count is reached. It automatically reloads the sample count at the next trigger. A special method is available for non-stop continuous sampling beyond 65K samples (select mode 4 and DO NOT write the counter registers).

Counter 1 determines the A/D clock rate using a 1MHz internal clock or external sample clock.

Counter 2 determines the internal trigger rate between scans or data frames using a 31.25kHz internal clock.

Control Word Register (Read/Write BASE + 7)

7	6	5	4	3	2	1	0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Select Counter	SC1	SC0	
	0	0	Select counter #0
	0	1	Select counter #1
	1	0	Select counter #2
	1	1	Read back command
Read/Load	RL1	RL0	
	0	0	Counter latch operation
	0	1	Read/Load LSB only
	1	0	Read/Load MSB only
	1	1	Read/Load LSB then MSB
Mode	M2	M1	M0
	x	1	0 Mode 2 rate generator
	1	0	0 Mode 4 software strobe
	1	0	1 Mode 5 hardware strobe
BCD	BCD		
	0		16-bit binary count
	1		4-decade binary coded decimal count

DAC 0 LOW BYTE (Write BASE + 8)
DAC 1 LOW BYTE (Write BASE + 10)
DAC 2 LOW BYTE (Write BASE + 12)
DAC 3 LOW BYTE (Write BASE + 14)

7	6	5	4	3 2 1 0
DA 9	DA 10	DA 11	DA 12 LSB	Not Used

DAC 0 HIGH BYTE (Write BASE + 9)
DAC 1 HIGH BYTE (Write BASE + 11)
DAC 2 HIGH BYTE (Write BASE + 13)
DAC 3 HIGH BYTE (Write BASE + 15)

7	6	5	4	3	2	1	0
DA 1 MSB	DA 2	DA 3	DA 4	DA 5	DA 6	DA 7	DA 8

DAC data is left justified. With the ±5V bipolar output range, the MSB is used for polarity (0 = negative, 1 = positive).

In single-channel mode (BASE + 2 bit 7 = 0), write the high data byte last to update all DAC outputs.

A/D CODING TABLE

Input (unipolar)	Input (bipolar)	Output Code (Hex)
+Full scale –1 LSB	+Full scale –1 LSB	FFF0h
1/2 FS +1 LSB	+1 LSB	8010h
1/2 full scale	Zero	8000h
1/2 FS –1 LSB	–1 LSB	7FF0h
Zero	–Full scale	0000h

ANALOG SIGNAL CONNECTORS

Pin numbering is shown as viewed from rear panel. (Channel addresses use single-ended/differential notation.)

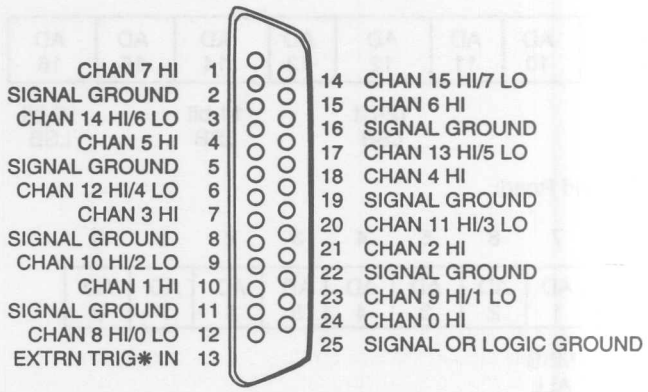


Figure 2. Analog Inputs, P1

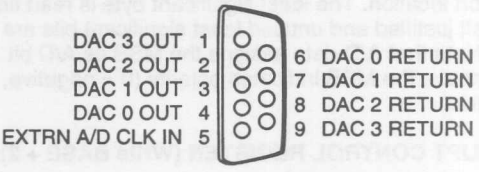


Figure 3. Analog Outputs, P2

ORDERING GUIDE

Model	A/D Bits	A/D Converter Sample Time	D/A Channels
PC-411A	12	7µs	none
PC-411B	14	14µs	none
PC-411C	16	32µs	none
PC-412A	12	7µs	4
PC-412B	14	14µs	4
PC-412C	16	32µs	4

Each board is power-cycle burned-in, tested and calibrated. All models include a user's manual. The warranty period is one year. Free QuickBASIC disk on request.

PC-411SET Set up and configuration program. Saves data to disk or memory buffer. Offers calibration and self test. Supplied on MS-DOS 3.5" disks. Documentation is in the user manual.

PC-411SRC Source code to PC-411SET on 3.5" MS-DOS diskettes. Includes "C" and assembly listings and window library.

PC-412LV Bridge driver library to National Instruments' LabVIEW (see PC-412LV data sheet).

PC-440 Expansion MUX board, 32SE/16D channels.

PC-490A/B Screw termination and cable, 490A is 9-pin, 490B is 25-pin.

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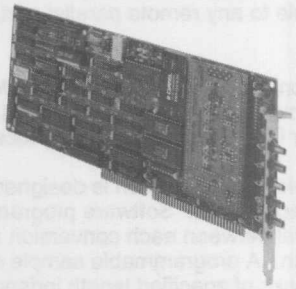
DATEL®
INNOVATION and EXCELLENCE

PC-414
High-Speed, Analog Input Board for ISA or EISA Computers

FEATURES

- **Up to 10MHz A/D sample rate**
- **Very low harmonic distortion**
- **Analog input comparator trigger**
- **Choice of 12 or 14-bit A/D resolution**
- **Optional 2 to 16-channel simultaneous sampling**
- **On-board FIFO memory up to 16,384 samples**
- **Ideal for FFT's, DSP or array-processor "front ends"**
- **Non-bus burst parallel port for seamless recording**

Now with LabVIEW® VI's



GENERAL DESCRIPTION

Offering very high system speed, the PC-414 is a multi-channel analog input board for ISA, EISA and compatible computers. A common motherboard is used, with the analog section contained in a pluggable 2" by 4" module. This allows for a family of several different Sample/Hold - A/D Converter speed and resolution options by exchanging analog modules. A/D resolutions are 12 or 14 bits, and sampling rates run as high as 10MHz.

The analog input ranges of the A/D converter are selectable as unipolar 0 to +10V, or bipolar ±5V, or ±10V depending on model. The gain on the PC-414A may be user-selected times one or times ten for two channels. This offers one-volt input ranges for receiver signal measurement. The input configuration is excellent for analyzing wide band communications signals. Model PC-414E offers 16 single-ended or 8 differential high speed channels.

Models PC-414A, F, G, and J use a Simultaneous Sampling section. This function acquires signals on parallel channels at the same time. This provides phase correction and deskewing of multichannel correlated signals. Applications include high-speed cross-channel computation, beam-former coherency for sonar or acoustics, telemetry, multiple carrier demodulation, and highly concurrent system testing.

A/D data passes to an on-board First-In, First-Out (FIFO) data memory and then to the host computer bus interface under software control. The FIFO acts to decouple the precise timing of the A/D section with the block-oriented data transfers on the bus. The design can continuously collect analog data with non-stop converter triggering while data is simultaneously read from the FIFO. This allows the collection of "seamless" wide-bandwidth signals of millions of samples or greater. Functions such as FFT sampling cannot tolerate lost samples without increases in "arithmetic" noise during computation processing.

Data may be transferred to mass storage peripherals such as disk or magnetic tape. Applications include long-baseline studies in astrophysics, component life testing, and anomalous pattern search.

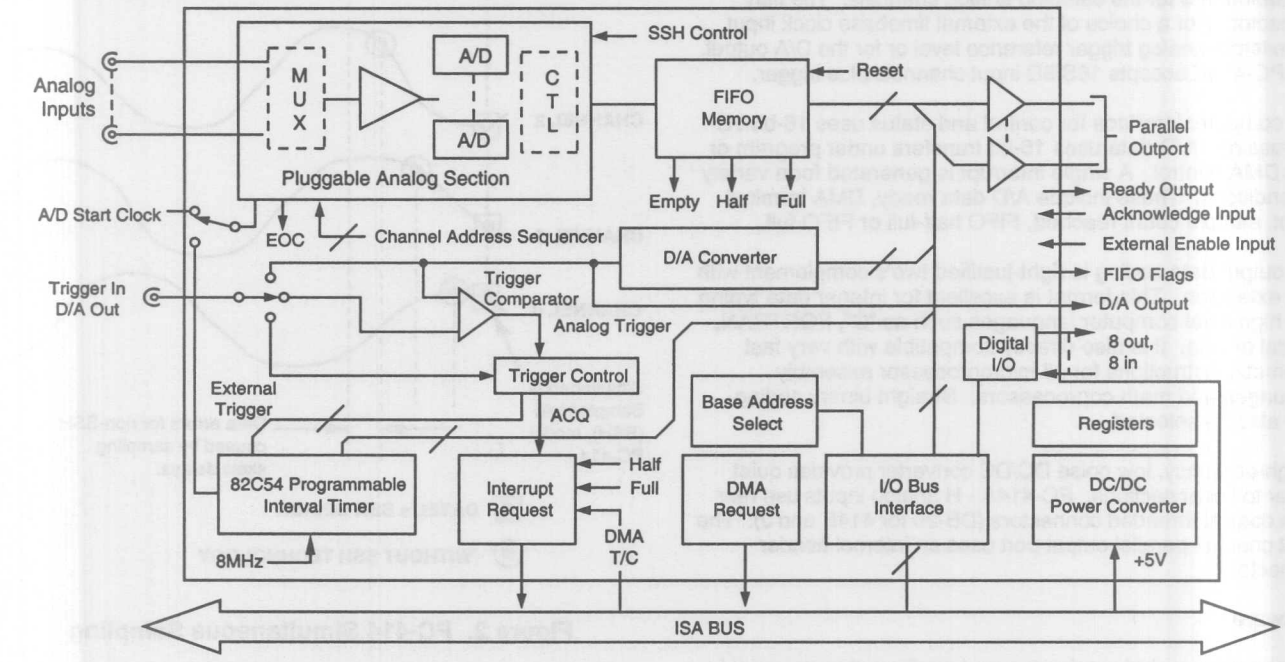


Figure 1. PC-414 Block Diagram

LabVIEW is a trademark of National Instruments
IBM is a trademark of IBM Corp.
DT Connect is a trademark of Data Translation
MS-DOS is a trademark of Microsoft

The FIFO data output may also be routed under host software control to an on-board parallel data port instead of being sent to the computer bus. This parallel burst channel data may be read by an external processor at very high speeds and avoids possible speed restrictions of the computer bus. The outport uses a very simple ready/acknowledge transfer handshake which is adaptable to any remote parallel port including DT Connect®.

The analog section of the PC-414 is optimized for high signal quality and very low dynamic noise. The PC-414 is ideal as an FFT "front end" or DSP quantizer for array processors.

The A/D conversion timing section is designed for accurate multi-scan data acquisition. Software programmable timers control the interval between each conversion and each multichannel scan. A programmable sample counter will allow sample blocks of specified length independent of FIFO length. The timer/counter section uses a precision on-board crystal clock. Timeout and sample count activities may be monitored using I/O status registers and/or programmable interrupts. The interrupt method may be fully synchronized with software programmable DMA transfers directly to host computer memory.

S/H-A/D triggering may use several sources under software control. The internal timebase is the normal trigger source although single conversions or scans may be directly commanded by host I/O register writes. An external trigger clock may also be used to precisely synchronize sampling with external events. This external trigger may start a single multichannel scan or "N" multiple scans separated by programmable delays.

Analog sampling may also be level-triggered using an on-board analog comparator and an external level input. The reference trigger level to the comparator is derived from an on-board 12-bit D/A converter. If preferred, the D/A converter may also be used as an analog output channel for any purpose.

The PC-414 A thru H contains five signal connectors. Four connectors are for the sampled analog channels. The fifth connector is for a choice of the external timebase clock input, the external analog trigger reference level or for the D/A output. The PC-414E accepts 16S/8D input channels plus trigger.

The computer interface for control and status uses 16-bit I/O addressing. A/D data uses 16-bit transfers under program or host DMA control. A single interrupt is generated for a variety of conditions. These include A/D data ready, DMA terminal count, sample count reached, FIFO half-full or FIFO full.

A/D output data coding is right-justified two's complement with sign extension. This format is excellent for integer data typing with high level computer languages such as "C", FORTRAN, Pascal or Ada. It is also directly compatible with very fast arithmetic instructions for all microprocessor assembly languages and math coprocessors. Straight binary coding may also be selected.

A high-efficiency, low noise DC/DC converter provides quiet power to linear sections. PC-414A - H analog inputs use rear SMA coaxial threaded connectors (DB-25 for 414E and J). The burst channel parallel output port uses an internal header connector.

Software

A menu-driven windowed setup and configuration program is optionally available on both 5.25" or 3.5" MS-DOS disks. The program automatically adapts to the display type and mouse.

The program sets the I/O base address, interrupt and DMA systems, loads registers and D/A converter data, starts timers and saves data to disk or memory. The entire hardware configuration may be saved to disk. The software also includes A/D-D/A calibration procedures.

A/D data may be sent to base memory (below 640K) either by DMA, program transfer, or extended memory (above 1Mb). Disk data formats include binary integer, IEEE-754 binary floating point, and ASCII floating point (Lotus PRN format). The setup program is also available in source language format and includes fast assembly language modules which may be linked to user-written programs. Both WINDOWS and MS-DOS versions are available.

Users have three methods of implementing PC-414 software; the optional setup/configuration program, third party software or user-written code. Third party display and processing software offers graphic outputs, DSP functions such as FFT's and statistical analysis of data files. Third party packages will accept data by file transfer. A QuickBASIC disk is available at no charge for user modification.

Simultaneous Sampling

In Figure 2, four input signals are sampled at the same time using the PC-414A's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired, they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors from conventional sequential multiplexer scanning. The PC-414F, G, or J offers the same function at a higher speed using multiple simultaneous A/D's.

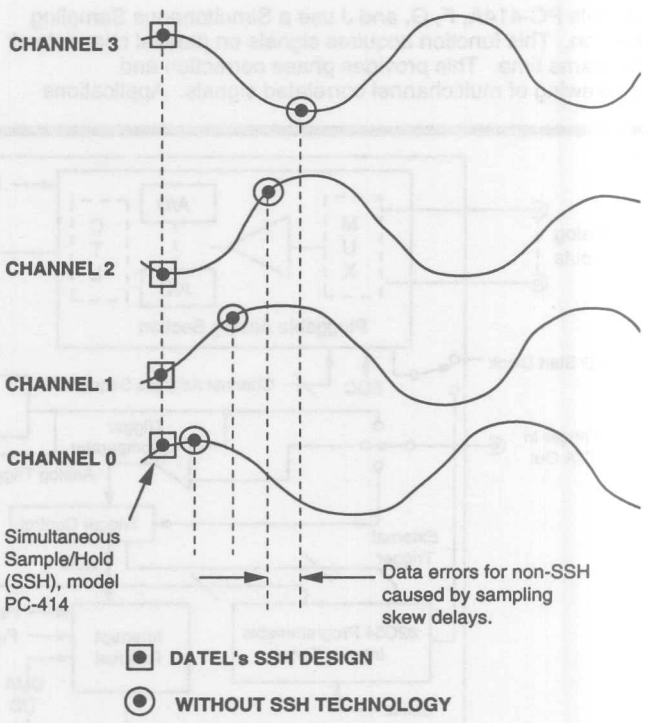


Figure 2. PC-414 Simultaneous Sampling

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FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	PC-414A	PC-414B	PC-414C	PC-414D	PC-414E
Number of Channels	4 Simultaneous	4	4	1	16S/8D
Input Configuration (non-isolated)	Single Ended	Single Ended	Single Ended	Differential	SE or Diff.
Full Scale Input Ranges (user-selectable)	0 to +10V ±10V	0 to +10V ±10V	0 to +10V ±10V	±5V	0 to +10V ±10V
(gain = 1)	[Footnote 1]	±5V	±5V		±5V [Footnote 1]
Input Bias Current	±1nA	±1nA	±1nA	±1nA	±1nA
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	2µs	2µs	2µs
Common Mode Voltage Range, maximum	—	—	—	±1V	±10V
Input Impedance [Footnotes 6 and 10]	10MΩ	10MΩ	10MΩ	2kΩ	100MΩ
SAMPLE/HOLD					
Acquisition Time (FSR step to 0.01% of FSR, max.)	900ns	750ns	200ns	50ns	750ns
Aperture Delay	15ns	20ns	20ns	10ns	20ns
Aperture Delay Uncertainty	±8ps	±100ps	±40ps	±7ps	±40ps
A/D CONVERTER					
Resolution	12 bits	14 bits	12 bits	12 bits	12 bits
Conversion Period	500ns	1.6µs	500ns	200ns	500ns
SYSTEM DC CHARACTERISTICS [Footnote 7]					
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1	±2	±1
Differential Non-linearity (LSB of FSR)	±0.75	±1	±0.75	±1	±0.75
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.1	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.3	±0.1
SYSTEM DYNAMIC PERFORMANCE [Footote 2]					
System Bandwidth (single channel, FSR input) [Footnote 12]	500kHz	200kHz	1MHz	2.5MHz	200kHz
Throughput to FIFO (single channel, gain = 1)	1.4MHz	500kHz	1.6MHz	5MHz [Footnote 9]	2MHz
Throughput to FIFO (sequential channels, gain = 1) [Footnote 4]	1MHz	330kHz	500kHz	—	500kHz
Total Harmonic Distortion [Footnote 3]	–72dB	–75dB	–72dB	–68dB	–72dB

ANALOG INPUTS	
Programmable Gains	See Note 1
Common Mode Rejection (DC - 60Hz)	-80dB (g = 100) (414E)
Addressing Modes	1. Single channel 2. Simultaneous sampling 3. Sequential with autosequenced addressing 4. Random addressing by host software

A/D CONVERTER	
Output Coding	Positive-true, right-justified, straight bin. (unipolar) or right-justified 2's comp. (bipolar) with sign extension thru bit 15
Trigger Sources (Software selectable)	1. Local Pacer frame clock 2. External TTL frame clock 3. Analog threshold comp.
A/D Sample Clock (software selectable)	1. Internal programmable 82C54 timer 2. Ext. TTL input, active low

FUNCTIONAL SPECIFICATIONS CONTINUED

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	PC-414F	PC-414G	PC-414H	PC-414J
Number of Channels	2 Simultaneous	2 Simultaneous	1	8 Simultaneous
Input Configuration (non-isolated)	Single Ended	Single Ended	Differential	Single Ended
Full Scale Input Ranges (user-selectable) (gain = 1)	0 to +10V ±5V	±5V or 0 to +10V (separate models)	±5V (other ranges special order)	0 to +2.5V, ±5V, ±10V (separate unipolar & bipolar models) [13]
Input Bias Current	±1nA	±1nA	—	±50nA (unipolar version)
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	1µs	3µs
Common Mode Voltage Range, maximum	—	—	±1V	—
Input Impedance [Footnotes 6 and 10]	1kΩ	1MΩ	2kΩ	8kΩ (bipolar)
SAMPLE/HOLD				
Acquisition Time (FSR step to 0.01% of FSR, max.)	165ns	350ns [Footnote 11]	35ns	400ns
Aperture Delay	20ns	20ns	±10ns	—
Aperture Delay Uncertainty	±40ps	±70ps	3ps rms	—
A/D CONVERTER				
Resolution	12 bits	14 bits	12 bits	12 bits
Conversion Period	400ns	500ns*	100ns	2µs (all chans. in simul. sampling)
SYSTEM DC CHARACTERISTICS [Footnote 7]				
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1.5	±1 max.
Differential Non-linearity (LSB of FSR)	±1	±1	±1	±1 max.
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 13]
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 13]
SYSTEM DYNAMIC PERFORMANCE [Footnote 2]				
System Bandwidth (single channel, FSR input) [Footnote 12]	1MHz	500kHz	5MHz	100kHz
Throughput to FIFO (single channel, gain = 1)	2MHz	1MHz*	10MHz	400kHz
Throughput to FIFO (multiple channels, gain = 1) [Footnote 4]	2MHz/chan. (2 chans.)	1MHz/chan.** (2 chans.)	—	2MHz (250kHz/chan., 8 simul. chans.)
Total Harmonic Distortion [Footnote 3]	–70dB	–80dB	–65dB	–77dB

*Dual 2MHz/channel 14-bit sampling is available on special order.

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A/D MEMORY	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024, 4096, or 16,384 A/D samples
TRIGGER CONTROL	
Programmable Interval Timer Type	82C54
Functions	1. A/D sample count reached 2. A/D start rate (16 bit divisor) 3. SSH sample counter (414A)
Pacer Sample Counter	3 to 65,536 samples. Drives the Acquire flag/interrupt gate for A/D start pulses.
82C54 Clock Source	Internal 8MHz crystal clock
Scan Trigger Clock	125, 250, or 500kHz
Analog Trigger Input Range [Note 5]	±10 Volts (not avail. 414D)
Analog Trigger Response	2µs to set status flag
Analog Trigger Hysteresis	40mV
ANALOG OUTPUT (not available PC-414D)	
Number of Channels	One channel
Function (user-selectable)	1. General purpose analog output 2. Threshold comparator for A/D trigger
Resolution	12 bits
Output Voltage Range (user-selectable)	0 to +10V, ± 5V and ±10V at 5mA max.
Linearity	± 0.05% of FSR
Settling time (10V step)	5 microseconds to 0.05%
Input Coding (user-selectable)	Same as A/D section
ISA BUS INTERFACE	
Architecture	I/O mapped, pluggable to IBM-PC/AT, PS-30, EISA bus and compatibles. Decodes eight 16-bit I/O registers.
I/O Mapping	Decodes I/O address lines A9-A0
Data Transfer	I/O transfer or host DMA, software selectable.
Data Bus	16 bits
Direct Memory Access	1 channel, selectable on channels 5, 6, or 7, set by software.
DMA Request Conditions (software selectable)	FIFO full, half full, not empty, scan acquire flag (sample count reached)
Control/Status Functions	Board reset, FIFO flags, interrupt select and status, DMA select and status, trigger source, timer control and period, sample count load, parallel outport enable, A/D enable, MUX auto-sequence
Number of Interrupts	1 interrupt, selectable on level 7, 9 thru 11, or 15. The interrupt level is set by software.
Bus Interrupt Sources	Scan acquire flag (sample count), FIFO full or half full, DMA terminal count from bus.

PARALLEL DATA PORT	
Outport Type	16 data output lines, TTL levels from A/D FIFO. Includes handshake signals and FIFO flags. The outport does not provide addressing.
Operating Modes	Asynchronous master to external slave receiver. 4 modes are included, offering internal/external clocking (to 10MHz), synchronous/ asynchronous handshaking. Sequencing is compatible with DT Connect®.
Parallel Port Loading	24mA out, 1.6mA in. The data outputs may be 3-stated for shared bus connection.
Parallel Port Connector	2-row 26-pin header type mounted on board interior. 0.100" pin spacing suitable for flat cable. Pinout is compatible with DT Connect® and existing 414 format.
Port Data Rate	4MHz maximum. Data may be transferred up to 10MHz with external clocking
DIGITAL I/O PORT	
Connector	Dual row, 26-pin header mounted on board interior. Uses 0.100" pin spacing suitable for flat cable. Includes +5V dc and digital ground connections.
Configuration	8 digital outputs, 8 digital inputs (unlatched)
Levels	All lines are buffered, TTL levels. 10 output loads.
Outport Settling Time	50ns max. after write operation
MISCELLANEOUS	
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain per channel for SSH on PC-414A,F,G. A single offset and gain pot is provided on PC-414B,C,D,E. Recommended recalibration interval is 90 days in stable conditions.
Analog Input Connectors	Four SMA miniature coaxial, mounted on rear slot. [Note 8]
Multipurpose Connector [Note 8]	5th SMA user-selectable for: 1. Pacer trigger input 2. Analog threshold comparator input 3. D/A output
Operating Temp. Range	0 to + 60°C
Storage Temp. Range	-25 to +85°C
Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet. Forced cooling is recommended.
Power Required	+5V @ 3.5A max. from ISA bus
Outline Dimensions	4.5 x 10.5 x 0.625 inches, compatible to PC/ISA bus

TECHNICAL NOTES

1. Resistor-programmed gain from X1 to X100 is available on PC-414E with increased settling delay at higher gain. Fixed gains of X1 and X10 on 2 channels, offering 1V ranges, are selectable on the PC-414A.

2. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion, and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

3. THD test conditions are:
   1. Input freq. 500kHz (414A,F) 200kHz (414B,E)
      300kHz (414C) 1MHz (414D)
      100kHz (414G)
   2. Generator/filter THD is -90dB minimum.
   3. THD computed by FFT to 5th harmonic.

$$THD = 20 * \log 10 \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}$$

   4. Inputs are 1/2 full scale. No channel advance.
   5. A/D trigger rate = 1.5MHz (414A), 500kHz (414B,C,E), 4MHz (414D), 2MHz (414F), 1MHz (414G)

4. The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the PC-414C were scanned, the maximum sample rate on any one channel would be 2µs X 4 channels = 8µs (125kHz per channel).

5. For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10V.

6. The input impedance of 10MΩ minimum avoids attenuation errors from external input source resistance. For many applications, an in-line coaxial 50 Ohm shunt, inserted adjacent to the front connectors, is recommended to reduce reflections and standing wave errors.

7. Allow 20 minutes warmup time to rated specifications for models PC-414B, G.

8. A 25-pin DB-25S connector is used for the PC-414E.

9. 5MHz sampling on PC-414D requires an external clock. Maximum on-board sampling is 4MHz.

10. Input impedance is shown with power on. Impedance with power off is 1500 Ohms or less.

11. PC-414G acquisition time is 350ns to ±0.01% of FSR.

12. Full power bandwidth is shown at approximately 3% distortion level. This is not the –3dB amplitude response which is at a higher but non-Nyquist frequency.

13. PC-414J bipolar input is user-selectable ±5V or ±10V per channel (default). Unipolar model is 0 to +2.5V. Total gain error over temperature range is ±4 LSB maximum. Total zero/offset error over temperature range is ±4 LSB maximum. Monotonicity: no missing codes over temperature range.

FIFO DATA FORMAT

A/D data is delivered as a stream from the FIFO memory. For multichannel inputs, this means that data is multiplexed. For example, for 4-channel inputs, the output channel sequence is 0, 1, 2, 3, 0, 1, ... Some applications may need this data de-multiplexed by software so that each channel's data is placed in its own separate buffer.

PC-414SET Setup/Configuration Software

- Automatically configures to the display adapter, CPU, and mouse
- Sets the I/O base address
- Initializes the interrupt and DMA systems and D/A output
- Allocates base or extended memory
- Performs self-test and A/D-D/A calibration
- Configures A/D sample rate, frame rate, and sample counter
- Selects trigger mode and DMA or I/O block transfer
- Selects disk file output format to integer binary, float binary, or ASCII float
- Saves data to base memory, extended memory, or disk
- Full source code in "C" and assembly is available
- MS-DOS or WINDOWS version (visual "C" interface)

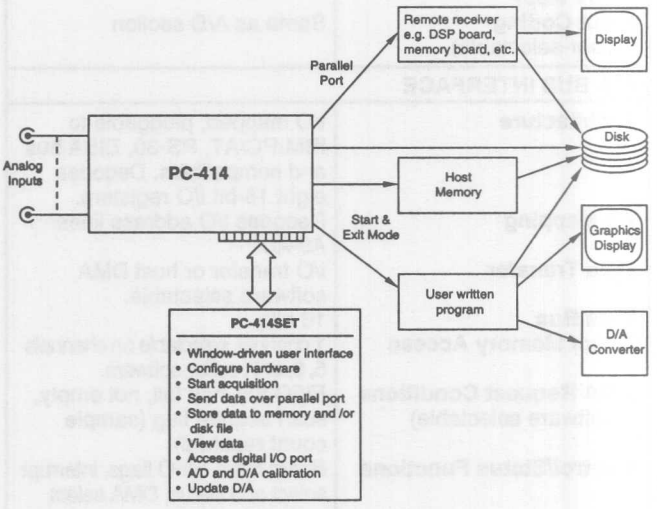


Figure 3. PC-414SET Software Operation

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I/O Register Mapping

The base address may be selected anywhere up to 3F0h on 16-byte boundaries.

I/O Address (hex)	Direction	Description
Base + 0	Write	Command Register
Base + 0	Read	Status Register
Base + 2	Write	Channel Address/Digital Output [Note 12]
Base + 2	Read	Digital Input Register [Note 12]
Base + 4	Write	D/A Data Register
Base + 6	Write	FIFO Reset Register
Base + 6	Read	FIFO A/D Data Register
Base + 8	Read/Write	Counter #0 (82C54)
Base + 0Ah	Read/Write	Counter #1 (82C54)
Base + 0Ch	Read/Write	Counter #2 (82C54)
Base + 0Eh	Read/Write	Control Register (82C54)

At power-up or PC bus reset, all registers contain zeroes except the FIFO HF and FF bits. The registers may be programmed in any sequence as long as the command register is last. Use 16-bit I/O word operations. See User Manual for full details.

Command Register (Write BASE + 0)

15 14	13 12 11	10 9	8 7	6	5	4	3	2	1	0
DMA Lvl 1 0	Intrpt Lvl 2 1 0	DMA Req 1 0	Intrpt Req 1 0	Prt/ Bus	Clk Sel	Trg Pol	Aut Inc	Scn En	Cn En	Trg Src

Channel Address Register (Write BASE + 2)

15 - 8	7 6 5 4	3 2 1 0
Digital I/O R/W [Note 12]	Scan Control 3 2 1 0	Channel Address 3 2 1 0

Status Register (Read BASE + 0)

15 - 8	7	6 5 4	3	2	1	0
Not Used	Xfr In Pro	FIFO Status FF HF EF	Ovr Smp Err	Ana Trg Lvl	EOC Sts	ACQ Sts

D/A Data Register (Write BASE + 4)

15-12	11	10	9	8	7	6	5	4	3	2	1	0
x-x	DA1 MSB	DA2	DA3	DA3	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12 LSB

FIFO Reset Register (Write BASE + 6)

15	0
x	x

FIFO Data Register (Read BASE + 6)

15	14	13	12	11	00
S	S	S	S	MSB 12	LSB ALL

12-bit A/D data

15	14	13	00
S	S	MSB 14	LSB ALL

14-Bit A/D Data

82C54 Programmable Interval Timer

Refer to the PC-414 User Manual for detailed programming information.

Counter Register (Read/Write BASE + 8 - Counter #0)
(Read/Write BASE + 0Ah - Counter #1)
(Read/Write BASE + 0Ch - Counter #2)

15 8	7	6	5	4	3	2	1	0
x - x	C07	C06	C05	C04	C03	C02	C01	C00

Control Word Register (Read/Write BASE + 0Eh)

15 8	7	6	5	4	3	2	1	0
x - x	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Transfer Speeds

ISA bus transfer rates are host-dependent and should be determined by testing. For example, a 80386 Compaq operating at 33MHz achieved 800 nanoseconds instantaneous sample-to-sample timing to base memory using the REP INSW instruction. To optimize throughput, disable all possible interrupts. For higher speed continuous (non-stop) A/D sampling, consider using a parallel port.

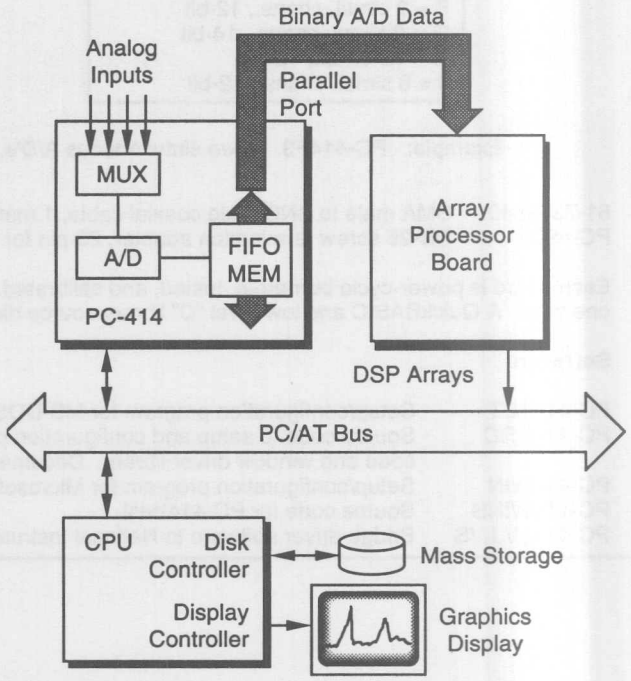


Figure 4. Array Preprocessing

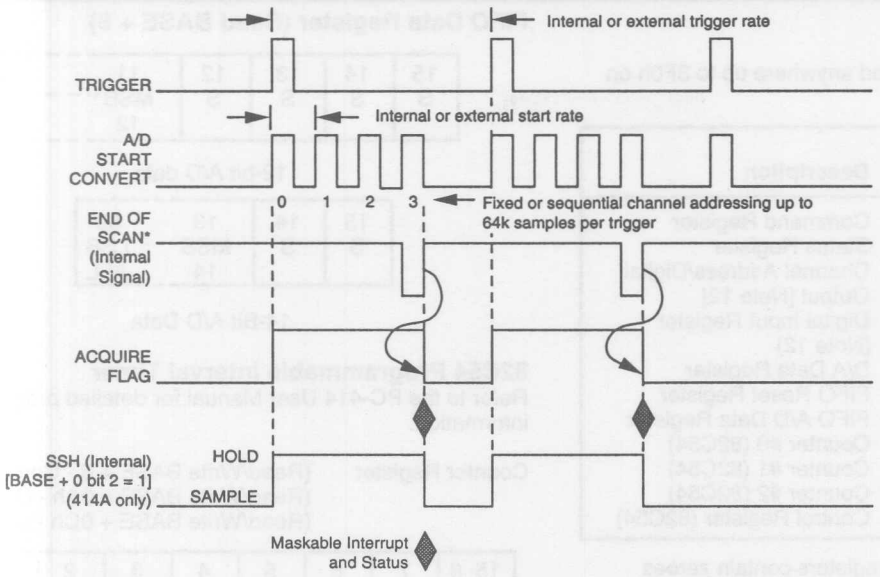


Figure 5.
PC-414 Timing Diagram

ORDERING INFORMATION

MODEL NUMBERING

Call DATEL for new analog modules

PC-414

A/D Type, Channels, Resolution	FIFO Memory Size	Input Polarity
A = 4 SE simul. chans., 12-bit B = 4 chans., 14-bit C = 4 chans., 12-bit D = 1D chan., 12-bit E = 16SE/8D chans., 12-bit F = 2 simul. chans., 12-bit G = 2 simul. chans., 14-bit H = 1D chan., 12-bit J = 8 simul. chans., 12-bit	1 = 1,024 A/D samples 2 = 4,096 A/D samples 3 = 16,384 A/D samples	A = Bipolar B = Unipolar Use this designator *only* for G and J models requiring polarity selection.

Example: PC-414F3 Two simultaneous A/D's, 2MHz, 12-bit resolution, 16,384 FIFO samples.

61-7342340 SMA male to BNC male coaxial cable, 1 meter length. (One cable required per channel)
PC-490B DB-25 screw termination adapter, 25-pin for PC-414E

Each board is power-cycle burned-in, tested, and calibrated. All models include a user's manual. The warranty period is one year. A QuickBASIC and low-level "C" library source disk is available on request at no charge.

Software:

PC-414SET	Setup/configuration program for MS-DOS. Includes executable files on MS-DOS disks.
PC-414SRC	Source code to setup and configuration program on MS-DOS disks. Includes "C" and assembly source code and window driver library. Documentation is on disk.
PC-414WIN	Setup/configuration program for Microsoft WINDOWS 3.1. Executables only.
PC-414WINS	Source code for PC-414WIN.
PC-414LV,LVS	Bridge driver software to National Instruments' LabVIEW. See PC-414LV data sheet.

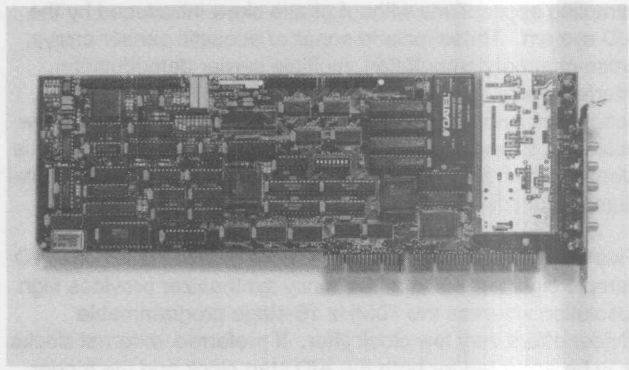
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DATEL®
INNOVATION and EXCELLENCE

PC-415
Ultra Fast A/D Boards for EISA Computers

FEATURES

- **Up to 10MHz A/D sampling rates**
- **Quick 32-bit EISA bus block transfers**
- **Wideband inputs with low harmonic noise**
- **12 or 14-bit A/D resolution**
- **2 to 16-channel simultaneous sampling**
- **On-board FIFO A/D memory to 8k samples**
- **Pre/post trigger "gap-free" ring buffering**
- **Compatible with Pentium® CPU's**
- **Ideal for FFT's, DSP's**
- **32 megasample streaming or greater**
- **Great array-processor "front end"**



GENERAL DESCRIPTION

Based on the 32-bit EISA bus (Extended Industry Standard Architecture), the PC-415 is an advanced performance data acquisition (A/D input) board family. The product accepts high-speed analog inputs, digitizes them into local FIFO (First In, First Out) memory and sends the data to the host EISA computer on program command. The entire system is optimized for continuous, non-stop, high-speed streaming of A/D samples to host memory or disk with no lost data. The design is excellent for a wide range of signal processing and data recording applications.

For very long baseline studies or high-speed transient capture, the PC-415 can collect greater than 64 megabytes of "seamless" digitized analog data to EISA memory. Typical EISA transfers are 14 megasamples per second in a mode C DMA (Direct Memory Access) 1k burst. Each 32-bit transfer consists of two A/D words using a unique banked FIFO technique. The on-board FIFO memory can simultaneously load from the A/D and transfer to the EISA bus without losing samples. The FIFO acts to decouple the precise timing of the A/D from the block bursts on the EISA bus.

The PC-415 offers extensive automated operation to reduce the amount of servicing required by the host PC. Most functions are fully software programmable. All analog channel addressing is either single channel or automatic sequential addressing with channel wrap-around at channel 3, 7 or 15. The board consists of a pluggable analog input section, FIFO memory, trigger and clock systems, EISA interface, interrupt/DMA sections, analog output, digital I/O, fast parallel data port and low-noise DC power conversion.

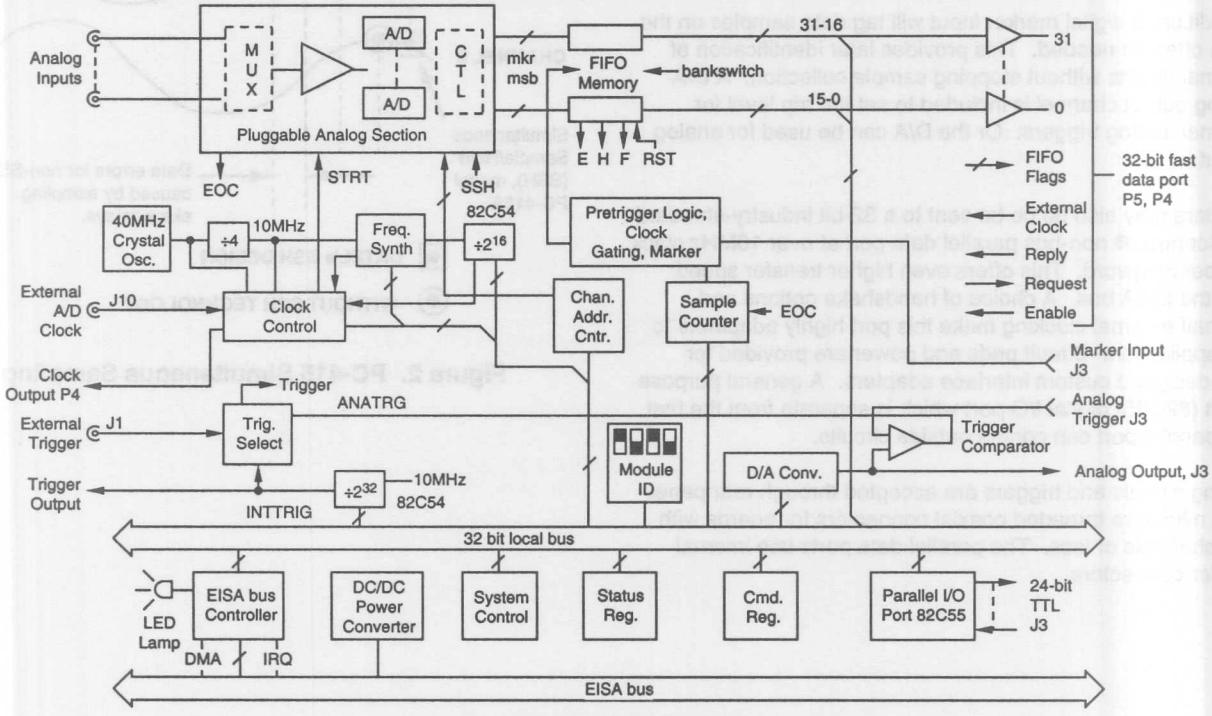


Figure 1. PC-415 Simplified Block Diagram

IBM is a trademark of the IBM Corp.
Pentium is a trademark of Intel
Windows is a trademark of Microsoft Corp.
DT Connect is a trademark of Data Translation

Several different pluggable analog options offer up to 16 channel inputs, multiple input ranges, single-ended/ differential, sample rates to 10MHz, 12- or 14-bit A/D resolution and various simultaneous sampling choices up to 8 channels. The simultaneous feature is intended for parallel sampling applications without phase skew introduced by the A/D system. These include sonar or acoustic sensor arrays, cross-channel computation, multiple carrier demodulation, interferometry, multichannel spectrometers, and highly concurrent system testing. High quality, wide bandwidth, low noise A/D's, and analog components are used. The design is ideal as an array processor "front end" or for DSP/FFT (Digital Signal Processing/Fast Fourier Transform) usage.

Two on-board software programmable timebases run the A/D sample clock. A 40MHz frequency synthesizer provides high resolution whereas the 10MHz 16-stage programmable divider offers very low clock jitter. If preferred, external clocks may be accepted for both the A/D start clock and the trigger. And several PC-415's may be connected in master-slave clocking for many simultaneous channels. A programmable 24-bit sample counter will collect long blocks up to 16 million samples. The trigger system can collect one fixed length frame, N repeating frames separated by programmable delays or can run "forever". Interrupts to EISA bus are programmable from the FIFO flags or the sample counter.

System features optimize gapless sampling without data loss. A pretrigger system can collect data continuously to host circular memory (ring buffer) of several megabytes or more. When an external trigger is received, the PC-415 will count down the number of preloaded post-trigger samples then automatically stop when all samples are collected. The trigger sample may then be found using a negative circular offset into the ring buffer, knowing the post-trigger sample count.

In addition, a digital marker input will tag data samples on the fly as often as needed. This provides later identification of external events without stopping sample collection. A D/A analog output channel is included to set the trip level for external analog triggers. Or the D/A can be used for analog output.

A/D data may also be be be sent to a 32-bit industry-standard DT Connect I® non-bus parallel data port at over 10MHz clock rate per longword. This offers even higher transfer speed than the EISA bus. A choice of handshake options and internal/ external clocking make this port highly adaptable to any application. Circuit pads and power are provided for user-designed custom interface adapters. A general purpose 24-bit (82C55) digital I/O port which is separate from the fast A/D parallel port can control outside circuits.

Analog signals and triggers are accepted through rear panel SMA miniature threaded coaxial connectors for boards with four channels or less. The parallel data ports use internal header connectors.

A menu-driven "no-programming" fast data recording system to memory or disk is available in the PC-415SET software. This "SET" software can also be obtained in source code format to modify the system. The PC-415 may be programmed in any language which can access 32-bit EISA I/O ports. For highest speed, the optimized "C" and assembly code is used under MS-DOS.

Simultaneous Sampling

In Figure 2, four input signals are sampled at the same time using the PC-415A's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired, they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors form conventional sequential multiplexer scanning. The PC-415F, G, or J offer the same function at a higher speed using two to 8 simultaneous A/D's.

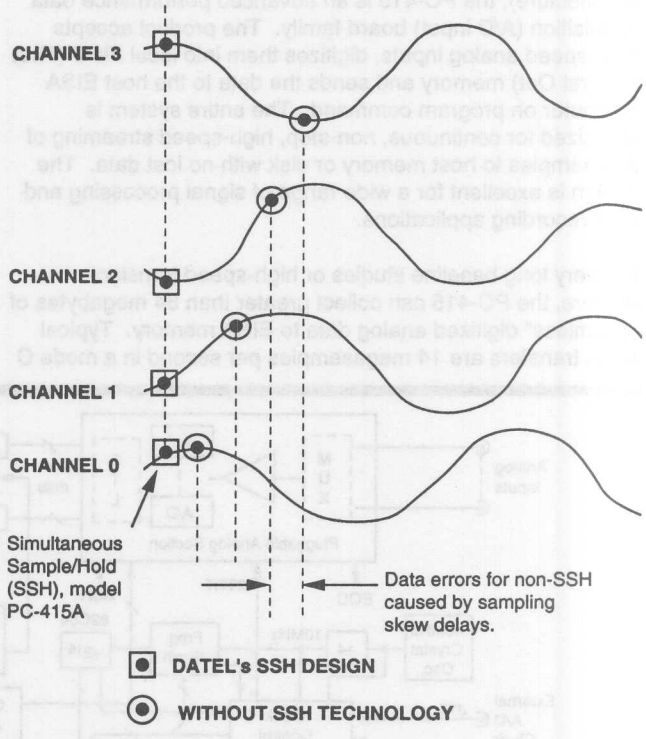


Figure 2. PC-415 Simultaneous Sampling

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FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	PC-415A	PC-415B	PC-415C	PC-415D	PC-415E
Number of Channels	4 Simultaneous	4	4	1	16S/8D
Input Configuration (non-isolated)	Single Ended	Single Ended	Single Ended	Differential	SE or Diff.
Full Scale Input Ranges (user-selectable) (gain = 1)	0 to +10V ±10V [Footnote 1]	0 to +10V ±10V ±5V	0 to +10V ±10V ±5V	±5V	0 to +10V ±10V ±5V [Footnote 1]
Input Bias Current	±1nA	±1nA	±1nA	—	±1nA
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	2µs	2µs	2µs
Common Mode Voltage Range, maximum	—	—	—	±1V	±10V
Input Impedance [Footnotes 6 and 9]	10MΩ	10MΩ	10MΩ	2kΩ	100MΩ
SAMPLE/HOLD					
Acquisition Time (FSR step to 0.01% of FSR, max.)	900ns	750ns	200ns	50ns	750ns
Aperture Delay	15ns	20ns	20ns	10ns	20ns
Aperture Delay Uncertainty	±8ps	±100ps	±40ps	±7ps	±40ps
A/D CONVERTER					
Resolution	12 bits	14 bits	12 bits	12 bits	12 bits
Conversion Period	500ns	1.6µs	500ns	200ns	500ns
SYSTEM DC CHARACTERISTICS [Footnote 7]					
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1	±2	±1
Differential Non-linearity (LSB of FSR)	±0.75	±1	±0.75	±1	±0.75
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.1	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.3	±0.1
SYSTEM DYNAMIC PERFORMANCE [Footote 2]					
System Bandwidth (single channel, FSR input) [Footnote 10]	500kHz	200kHz	1MHz	2.5MHz	200kHz
Throughput to FIFO (single channel, gain = 1)	1.4MHz	500kHz	1.6MHz	5MHz	2MHz
Throughput to FIFO (sequential channels, gain = 1) [Footnote 4]	1MHz	330kHz	500kHz	—	500kHz
Total Harmonic Distortion [Footnote 3]	–72dB	–75dB	–72dB	–68dB	–72dB

ANALOG INPUTS	
Programmable Gains	See Footnote 1
Common Mode Rejection (DC - 60Hz)	-80dB (g = 100) (415E)
Addressing Modes	1. Single channel 2. Simultaneous sampling 3. Sequential with autosequenced addressing 4. Random addressing by host software

A/D CONVERTER	
Output Coding	Positive-true, right-justified, straight bin. (unipolar) or right-justified 2's comp. (bipolar) with sign extension thru bit 15

FUNCTIONAL SPECIFICATIONS CONTINUED

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	PC-415F	PC-415G	PC-415H	PC-415J
Number of Channels	2 Simultaneous	2 Simultaneous	1	8 Simultaneous
Input Configuration (non-isolated)	Single Ended	Single Ended	Differential	Single Ended
Full Scale Input Ranges (user-selectable) (gain = 1)	0 to +10V ±5V	±5V or 0 to +10V (separate models)	±5V (other ranges special order)	0 to +2.5V ±5V, ±10V [13] (separate unipolar & bipolar models)
Input Bias Current	±1nA	±1nA	—	±50nA (unipolar version)
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	1µs	—
Common Mode Voltage Range, maximum	—	—	±1V	—
Input Impedance [Footnotes 6 and 9]	1kΩ	1MΩ	2kΩ	8kΩ (bipolar)
SAMPLE/HOLD				
Acquisition Time (FSR step to 0.01% of FSR, max.)	165ns	350ns	35ns	400ns
Aperture Delay	20ns	20ns	±10ns	—
Aperture Delay Uncertainty	±40ps	±70ps	3ps rms	—
A/D CONVERTER				
Resolution	12 bits	14 bits	12 bits	12 bits
Conversion Period	400ns	500ns*	100ns	2µs (all chans. in simul. sampling)
SYSTEM DC CHARACTERISTICS [Footnote 7]				
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1.5	±1 max.
Differential Non-linearity (LSB of FSR)	±1	±1	±1	±1 max.
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 13]
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 13]
SYSTEM DYNAMIC PERFORMANCE [Footnote 2]				
System Bandwidth (single channel, FSR input) [Footnote 10]	1MHz	500kHz	5MHz	100kHz
Throughput to FIFO (single channel, gain = 1)	2MHz	1MHz*	10MHz	400kHz
Throughput to FIFO (sequential channels, gain = 1) [Footnote 4]	2MHz/chan. (2 chans.)	1MHz/chan.* (2 chans.)	—	2MHz (250kHz/chan. 8 chans. simul.)
Total Harmonic Distortion [Footnote 3]	–70dB	–80dB	–65dB	–77dB

*Dual 2MHz 14-bit sampling is available on special order.

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SPECIFICATIONS, CONTINUED

(Typical @ +25°C, dynamic conditions, unless noted)

A/D SAMPLE CLOCK	
Sample Clock Sources	Selectable from among: 1. Frequency synthesizer 2. 10MHz crystal oscillator 3. 20MHz crystal oscillator 4. 16-stage binary divider to either 1 or 2, maximum input: 10MHz 5. External digital input
Frequency Synthesizer	Output 5-10MHz in 625Hz steps, further divisible by 16-stage binary divider, all software programmable. Up to 40MHz is available in 2500Hz steps.
Total Sample Range	76.3Hz to 10MHz (40MHz available)
Oscillator Frequency Accuracy	±50ppm (+20 to +30°C)
Crystal Aging	±5ppm/year

TRIGGER CONTROL	
Trigger Sources [Footnote 11]	1. Analog threshold comparator using internal D/A to set trip level 2. Internal trigger derived from10MHz timebase, divided by 32-stage divider (82C54). Range: 20ns to 429.5 seconds. 3. External digital trigger
Trigger Response	Selectable from among: 1. Starts one frame ("single trigger mode") 2. Collects repeating frames, each started by a trigger ("continuous trigger mode") 3. Runs the A/D "forever" (sample counter disabled)
A/D Samples per Frame	1 to 16,777,216 samples (24-bit counter) or "forever"
Analog Trigger Input Range	±10V
Analog Trigger Response	2µs [Footnote 5]
Analog Trigger Hysteresis	±40mV

ANALOG OUTPUT	
Number of Channels	One channel
Function	Selectable from among: 1. General purpose analog output 2. Threshold comparator for A/D trigger
Resolution	12 bits
Output Voltage Range	0 to +10V, ±5V, ±10V at 5mA max. (user selectable)
Linearity	±0.05% of FSR
Settling Time	5 microseconds (10V step)
Input Coding	Straight binary

EISA Bus	
Data Bus Size	32 bits
Address Bus Size	32 bits
EISA Controller Type	Hitachi HD64981F ESIC, bus slave mode
Spec. Conformance	EISA revision 3.12
Data Transfer	32-bit I/O or DMA mode A, B, or C (burst)
Direct Memory Access	One channel, selectable by software on channels 3, 5, 6, or 7. Terminal count appears as local status bit or EISA interrupt.
Interrupts	One interrupt, software selectable on level 10, 11, 12, or 15
Interrupt Sources	FIFO, half full sample count reached (ACQuire flag), DMA terminal count from bus

MISCELLANEOUS	
LED Lamp	Internal red light emitting diode, for diagnostics, controlled by ESIC DIP register bit
Board Identification Switch	4-bit DIP switch is factory preset to identify A/D module type. May be changed if another module is used.
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain per channel for SSH on PC-415A,F,G. A single offset and gain pot is provided on PC-415B,C,D,E. Recommended recalibration interval is 90 days in stable conditions.
Operating Temp. Range	0 to +60°C
Storage Temp. Range	–25 to +85°C
Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet, forced cooling is recommended
Power Required	+5V dc @ 4A max. from EISA bus
Outline Dimensions	4.5 x 13.31 x 0.625 inches, compatible to EISA bus

A/D MEMORY	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	2048 or 8192 A/D samples (other sizes on special order)

CONNECTORS	
EISA bus	Two edgeboard connectors with EISA slot
Analog Input (4 channels or less)	Four SMA miniature threaded coaxial, mounted on rear slot plate
Analog Input [Footnote 8] (more than 4 channels)	DB-25 25-pin connector mounted on rear plate
External Trigger [Footnote 12]	SMA miniature threaded coaxial on rear plate
External A/D Clock In	SMA miniature threaded coaxial on rear plate
Fast Parallel Data Port	Two 26-pin header connectors, P4 and P5. Mounted on board interior, suitable for flat cables.
Digital I/O Port	50-pin header connectors, P3. External clock, D/A mounted on board interior, suitable for flat cables.
DIGITAL I/O PORT	
Configuration	24 lines, programmable as input or output with latches and handshakes
Controller	82C55
Levels	TTL logic, 1 TTL load in or out (direct from 82C55)
Outport Settling Time	50ns, after write operation
PARALLEL DATA PORT	
Outport Type	32 data output lines, TTL levels from A/D FIFO. Includes handshake signals and FIFO flags. The outport does not provide addressing.
Operating Modes	Master or slave to external receiver. 4 modes are included, offering internal/external clocking (to 10MHz), synchronous/ asynchronous handshaking. Sequencing is compatible with DT Connect®.
Parallel Port Loading	24mA out, 1.6mA in
Parallel Port Connector	Two 26-pin header types, mounted on board interior. 0.100" pin spacing suitable for flat cable. Pinout is compatible with DT Connect®.
Port Data Rate (32 bits)	10MHz maximum external clock, or 5MHz internal clock

FOOTNOTES

1. Resistor-programmed gain from X1 to X100 is available on PC-415E with increased settling delay at higher gains. Fixed gains of X1 and X10 on 2 channels, offering 1V ranges, are selectable on the PC-415A.

2. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion, and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

3. THD test conditions are:
   1. Input freq. 500kHz (415A,F) 200kHz (415B,E) 300kHz (415C) 1MHz (415D) 100kHz (415G) 2MHz (415H)
   2. Generator/filter THD is -90dB minimum.
   3. THD computed by FFT to 5th harmonic.
      $$THD = 20\left(\log10\ \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}\right)$$
   4. Inputs are full scale –0.5dB. No channel advance.
   5. A/D trigger rate = 1.5MHz (415A), 500kHz (415B,C,E), 4MHz (415D), 2MHz (415F), 1MHz (415G), 10MHz (415H).

4. The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the PC-415C were scanned, the maximum sample rate on any one channel would be 2µs X 4 channels = 8µs (125kHz per channel).

5. For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10V.

6. The input impedance of 10MΩ minimum avoids attenuation errors from external source resistance. For many applications, an in-line coaxial 50 Ohm shunt, inserted adjacent to the front connectors, is recommended to reduce reflections and standing wave errors.

7. Allow 20 minutes warmup time to rated specifications for models PC-415B,G.

8. A 25-pin DB-25S connector is used for the PC-415E,J.

9. Input impedance is shown with power on. Impedance with power off is 1500 Ohms or less.

10. Full power bandwidth is shown at approximately 3% distortion level. This is not the –3dB amplitude response which is at a higher but non-Nyquist frequency.

11. Avoid mixing external triggers which are a close submultiple of the internal A/D start clock to prevent lost samples.

12. The 5th SMA connector may be dedicated to either external trigger or external A/D clock.

13. PC-430J bipolar input is user-selectable ±5V or ±10V per channel (default). Unipolar model is 0 to +2.5V. Total gain error over temperature range is ±4 LSB maximum. Total zero/offset error over temperature range is ±4 LSB maximum. Monotonicity: no missing codes over temperature range.

REGISTER I/O MAPPING

Many of the PC-415's registers require 32-bit I/O instructions. DATEL software provides examples and highly portable Assembly modules which can be used with any language. The PC-415 is compatible with mode C DMA burst transfers, which are the fastest available on EISA. All registers are fully described in the User Manual, included with the board.

I/O Address (Hex)	Direction	Access Size	Description
0zC00	Write	32 bits	Command register
0zC00	Read	32 bits	Status register
0zC04	Write	32 bits	Sample count register
0zC08	Write	16/32 bits	A/D channel address register
0zC08	Read	16/32 bits	Reset FIFO register
0zC0C	Write	16 bits	A/D convert enable register
0zC0C	Read	32 bits	FIFO A/D data register
0zC10	Write	16 bits	Phase lock loop registers
0zC20-23	Rd/Wr	8 bits	82C54 Timer/Counter registers
0zC30-33	Rd/Wr	8 bits	82C55 parallel port registers
0zC40	Write	16 bits	DAC data register
0zC80-CBF	Rd/Wr	8 bits	HD64981F EISA controller registers

Note: "z" is the EISA slot address

Marker Input

When selected in the Command Register the marker input is for tagging A/D samples to an external event such as a clock timebase. The marker sets bit 15 of the A/D word to logic "1" for one sample clock cycle. Lower A/D bits still retain sign extension polarity. This tag is now stored in the FIFO along with the A/D sample. The user may do this as often as needed and the marker can be asynchronous with the A/D sample clock. Post processing software then searches through the saved data to find each marked sample.

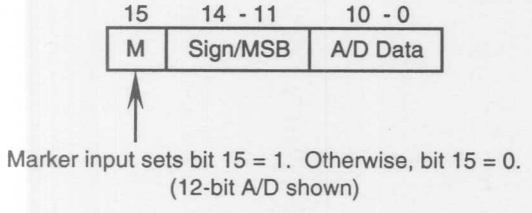
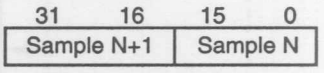


Figure 3. Marker Sample Tagging

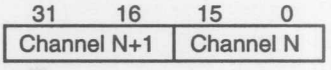
A/D Data Format

A/D data is delivered as a stream from the FIFO memory. For multichannel inputs, this means that data is multiplexed by the channel address with a modulo address wrap-around at the top channel. For example, with 4-channel inputs, the output channel sequence is 0, 1, 2, 3, 0, 1, . . . One additional factor is that the 32-bit wide dual FIFO contains two A/D samples. Therefore the longword sequence is 0,1 . . . 2,3 . . . 0,1 . . .

The FIFO output can take two formats depending on which analog module is used and whether single channel or autosequential (autoincrement) channel addressing is selected. For single channel mode, data appears as follows:



If the addressing is selected for autoincrement, data appears this way:



Note that all A/D data is right-justified within the 16-bit data word with sign extension to bit 15 or 31. Also be aware that the PC-415 uses "Intel" or little-endian addressing where lower (or earlier) data is lower in word memory.

PC-415SET SETUP/CONFIGURATION SOFTWARE

- Automatically configures to the display adapter, CPU, and mouse using the DATEL EISA configuration file.
- Initializes the interrupt and DMA systems and D/A output
- Allocates base or extended memory
- Performs self-test and A/D-D/A calibration
- Configures A/D sample rate, frame rate, and sample counter
- Selects trigger mode and DMA or I/O block transfer
- Selects disk file output format to integer binary, float binary, or ASCII float
- Saves data to base memory, extended memory, or disk
- Full source code in "C" and assembly is available
- MS-DOS or WINDOWS version (visual "C" interface)

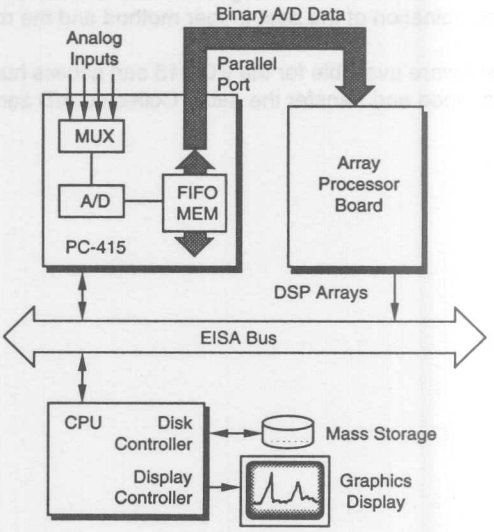


Figure 4. Array Preprocessing

Pre/Post Trigger Transient Capture Applications

A certain class of applications requires data sampled relative to one or more external events. Data before and after the event need to be analyzed. If the exact time of those external events cannot be predicted accurately but the event can be identified with a trigger, data must be recorded continuously then processed after the event occurred. At higher sample rates, the user must use all-memory storage which has limited capacity but is still large enough to capture the event. A ring buffer circular storage method is used where new samples continually overwrite the oldest samples.

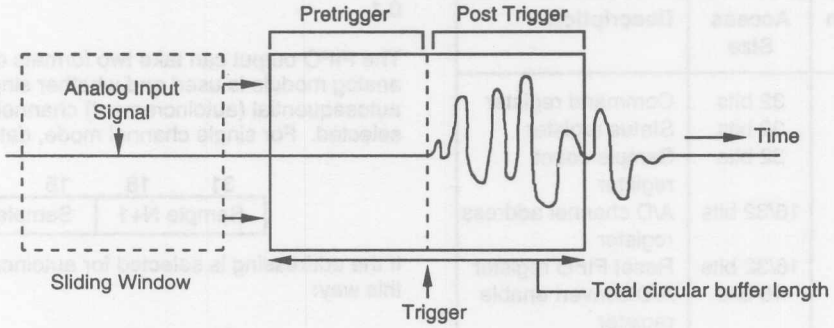


Figure 5. Transient Signal Capture

The PC-415 accepts either a digital or analog (threshold trip) event trigger. An on-board D/A converter sets the comparator voltage level for the analog trigger. The system stores data before and after the trigger. A post trigger sample counter selects the number of offset samples after the trigger. The number of pretrigger samples equals the total circular storage minus the post trigger size. Note that pretrigger samples in Figure 6 are skewed over the buffer tail.

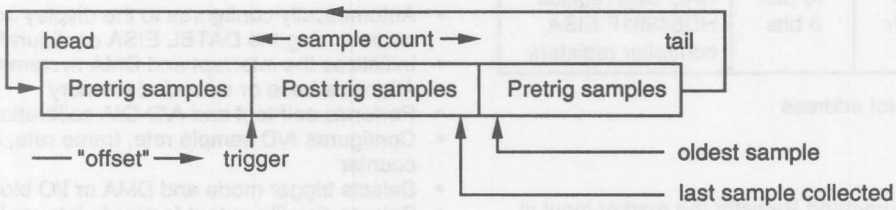


Figure 6. A/D Data Ring Buffering

A/D collection continues after the trigger until the system has stored the number of samples specified in the sample counter. The trigger sample can be found using backwards circular offset from the last sample saved. Multiple external events can be identified using a combination of the post trigger method and the marker inputs.

Special software available for the PC-415 can access huge EISA memory. This requires the 80486 or Pentium CPU to enter protected mode and transfer the data. Collected A/D samples can then be saved to disk or tape.

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Highly Parallel Array Sampling

Although the A, F, G, and J models of the PC-415 offer unique high performance simultaneous sampling capabilities, this can be extended by connecting several PC-415's in parallel. A master PC-415 can distribute its internal trigger signal to several other 415's for concurrent sampling with practically no phase lag. Applications include sensor arrays, astrophysics, biomedical sampling, engine cells, multichannel audio, and aerospace structure testing.

Two interconnection methods accommodate either externally or internally triggered applications. External triggers simply connect in parallel to all PC-415's. Each board is armed with its sample count and clocking systems to perform parallel sampling. Only one board sends interrupts. When data is ready, the host EISA system rapidly retrieves data blocks from each board in sequence.

For internal triggers, one board is the master generating triggers for itself and for all other boards. Slave 415's attach to the master 415's trigger output connection.

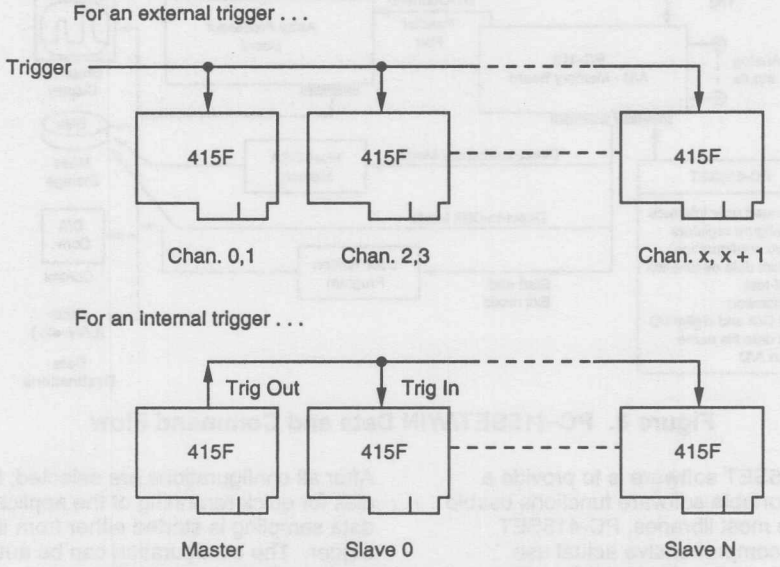


Figure 7. Highly Parallel Simultaneous Sampling

Trigger and Sample Count Systems

The PC-415 accepts one of three triggers - external analog, internal or external digital. All three initiate identical internal actions. For the internally generated trigger, either a single trigger can be accepted ("single trigger mode") or the trigger can repeat ("continuous trigger mode") with programmable delays between each trigger.

Internal trigger rates are independent from but synchronous to the internal programmable A/D clock rate. The trigger starts a frame of samples. Each frame can be from one to 16,777,216 samples using a 24-bit counter. The system will collect the number of samples in the sample counter then stop and wait for the next trigger. Meanwhile the sample counter will automatically reload in anticipation of the next trigger. Data flows into the FIFO memory which will notify the host that it has data to be saved. The FIFO size is independent of the frame size, therefore FIFO flags will occur separately from the sample counter.

An EISA bus interrupt can be generated after each frame completes (the "ACQuire" interrupt), or at each FIFO half full signal. Interrupt is also available after each DMA block transfer.

Three basic trigger modes are offered. A single trigger will start one frame then stop. The continuous trigger mode will generate repeating frames. In the last "forever" mode, the sample counter is disabled. A single trigger will start sampling indefinitely. The host computer must then externally decide when to stop sampling.

The PC-415 will automatically control its own channel addressing such that the address advances immediately as a sample is sent to the FIFO. In single channel mode, each frame will consist of data from only the selected channel. In automatic sequential addressing ("autoincrement"), the frame will contain one or more scans of channels, with addresses automatically wrapping around according to the channel capacity of the analog module.

The combination of programmable sample count, frame rate, A/D rate, and channel addressing mean that practically all conceivable applications can be done. The basic system timing is shown in Figure 11 on page 12.

PC-415 Software

DATEL's PC-415SET is a comprehensive stand-alone software program to configure and control the PC-415 board. The program serves two functions. It's primary mission is fast collection of digitized A/D data. It also shows how to write programs for the board.

After setting up the timer/counter trigger systems and all other registers, A/D samples are sent either to memory or direct to disk. The "memory first" mode is very fast but limited to the memory capacity. After sampling, filled memory is then saved to a file for later analysis.

In this direct-to-memory mode, the system can use large EISA memory over 64 Megabytes. Full 32-bit mode C (burst) DMA transfers are used for highest speed. Flags indicate if data is lost.

Another option is to send data directly to file. This direct-to-disk mode is considerably slower than memory mode but can use most of the disk capacity.

The overall data and command flow of PC-4156SET is shown below:

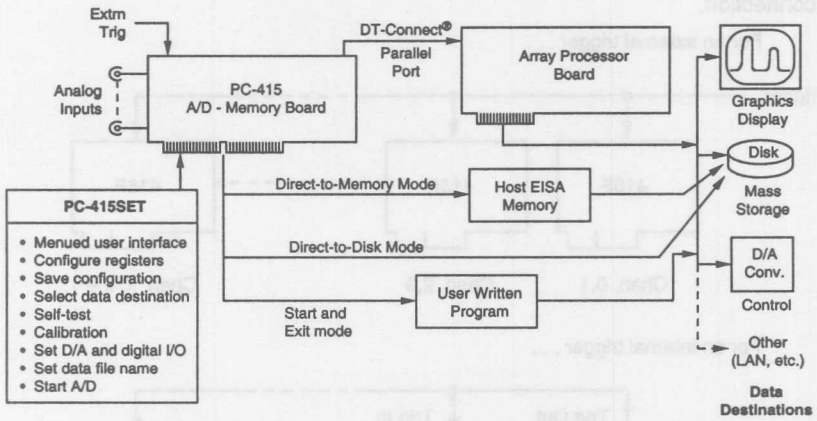


Figure 8. PC-415SET/WIN Data and Command Flow

A second purpose of PC-415SET software is to provide a library of fully-commented portable software functions usable in other applications. Unlike most libraries, PC-415SET shows the example code in comprehensive actual use. PC-415SET is written in Borland C++ Turbo Vision. The sources are professionally written, highly modular and heavily commented.

PC-415SET presents a series of menu screens selecting modes, timing, triggers, output destination, data filenames, number of samples and other parameters. The menu tree is selected by mouse or keyboard and the top level is shown in Figure 9.

After all configurations are selected, they may be saved to disk for quick rerunning of the application. When set, A/D data sampling is started either from the keyboard or the trigger. The configuration can be automatically rerun ("autorun") from a batch file.

As a data recorder, output data files use universal integer binary, ASCII float or binary (IEEE) float formats. The files can be analyzed and displayed with the user's choice of spreadsheets, graphic systems and signal display software. PC-415SET does not have any internal graphics display but instead uses the already extensive graphic display/process functions available with spreadsheets and signal analyzers. Many users have these tools and do not wish to learn different ones. The data files of course may also be processed by simple "C" or BASIC programs.

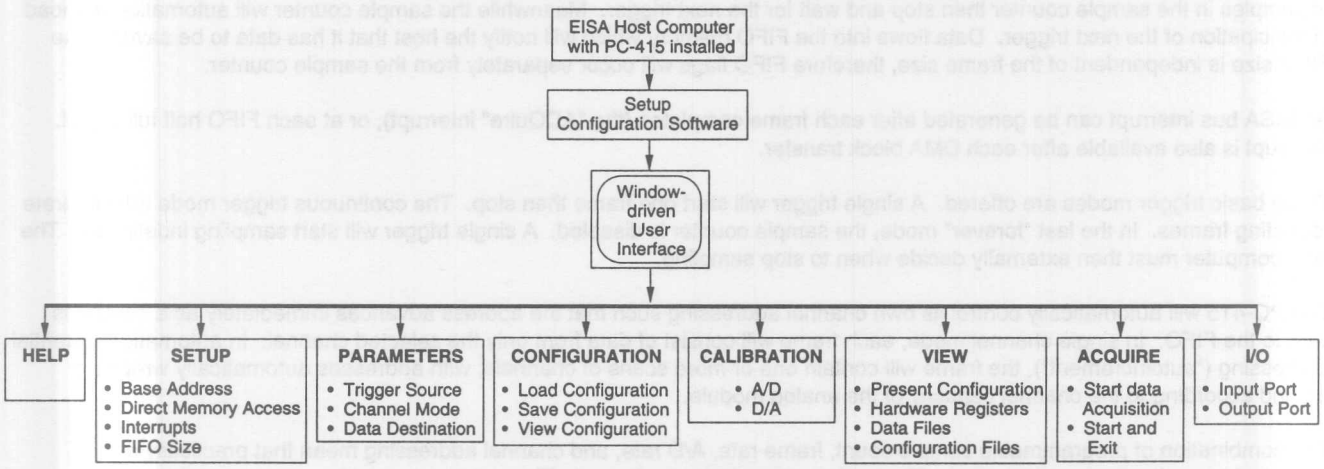


Figure 9. PC-415SET Opening Menu

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Start and Exit Mode

For applications which need the data streaming continuously to external software, the extensive library functions can easily be interleaved with user-written code. A special "start and exit" mode in PC-415SET simply configures the board via menues, starts A/D conversion then exits to the operating system without saving any data. Next, the user's following program (usually in a batch file) retrieves data directly from the on-board registers or via 32-bit DMA. This is simple to program and very high speed. This data collection program may loop back repeatedly to get fast blocks of data and the PC-415 continues filling the FIFO while the user program runs. This is true concurrent coprocessing with no lost data.

Start and exit mode offers a high degree of control over the board while avoiding time-comsuming menu design and coding. The system will even wait for an external trigger, giving time to set up the data collection program. Start and exit mode can be saved to automatically run, like all other PC-415SET applications. A typical program flow for start and exit is shown below:

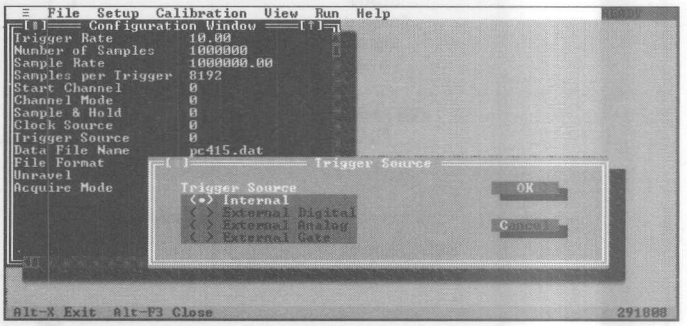


Figure 10. PC-415SET Menu Display

1. SETUP PC-415 board.
2. Save configuration to disk.
3. Start A/D and exit to MS-DOS (the A/D stays running).

<start of user's program>

LOOP:

4. If the FIFO overflowed, process the error.
5. Move block of A/D data from FIFO to host memory.
6. Do other processing on A/D data block (math, disk, display, etc.).
7. If more data is needed, GO TO LOOP.
8. Else, stop the A/D and quit.

The "Do other processing ..." step is a program written by the user. Notice that the PC-415 continues with non-stop A/D sampling during this step.

Besides being a fast data recorder, PC-415SET also performs register tests to verify proper board operation. In addition, PC-415SET does calibration using an external DC voltage source, loads data into the D/A channel and exercises the digital I/O port.

The source code may be modified by the user (or by DATEL under special order) to adapt to any conceivable function.

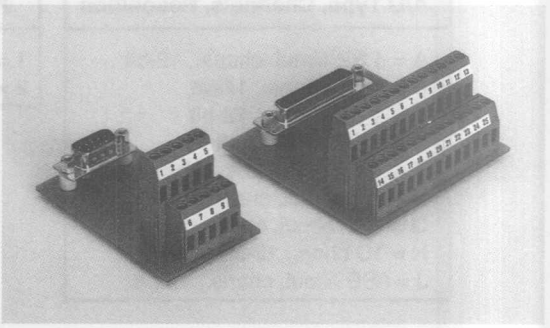


Figure 11. PC-490A and -490B D-Connector to Screw Terminal Adapters

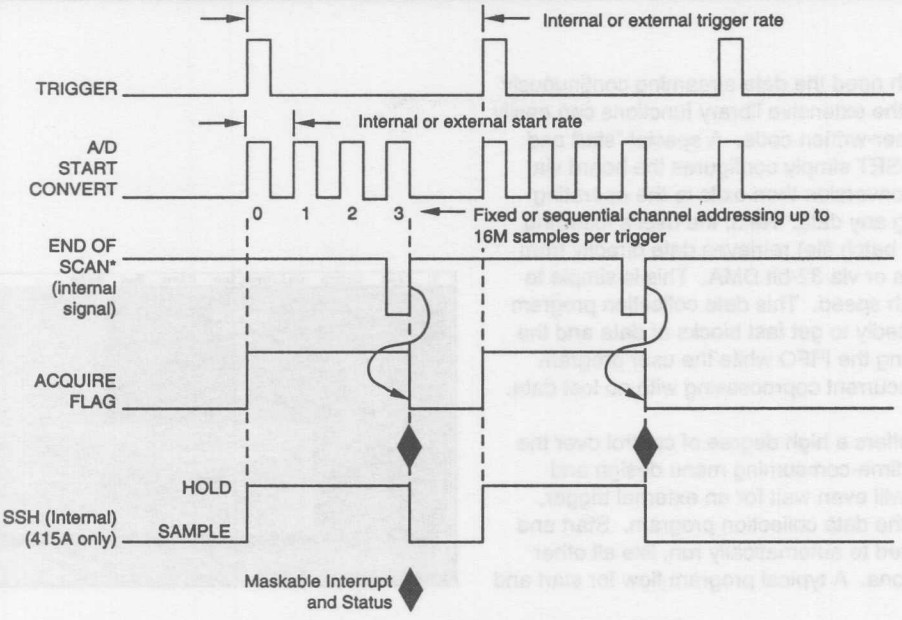


Figure 11. PC-415 Timing Diagram

ORDERING INFORMATION

PC-415 — — —

A/D Type, Channels, Resolution	FIFO Memory Size	Input Polarity
A = 4 SE simul. chans., 12-bit B = 4 SE chans., 14-bit C = 4 SE chans., 12-bit D = 1 D chan., 12-bit E = 16SE/8D chans., 12-bit F = 2SE simul. chans., 12-bit G = 2SE simul. chans., 14-bit H = 1D chan., 12-bit J = 8SE simul. chans., 12-bit	1 = 2k A/D samples 2 = 8k A/D samples	A = Unipolar B = Bipolar Use this designator *only* for G and J models requiring polarity selection.

Call DATEL for new analog modules

Example: PC-415J2B 8 simultaneous A/D's, 8k FIFO, ±5V input.

61-7342340 SMA male to BNC male coaxial cable, 1 meter length. (One cable required per channel)
PC-490B DB-25 screw termination adapter, 25-pin for PC-415E and J.

Each board is power-cycle burned-in, tested, and calibrated. All models include a user's manual. The warranty period is one year.

Software:

PC-415SET Setup/configuration program for MS-DOS. Includes executable files on 3.5" MS-DOS disks.
PC-415SRC Source code FOR PC-415SET Includes "C" and assembly source code. Documentation is on disk.
PC-415DRV Low level library and test program sources (included with board).

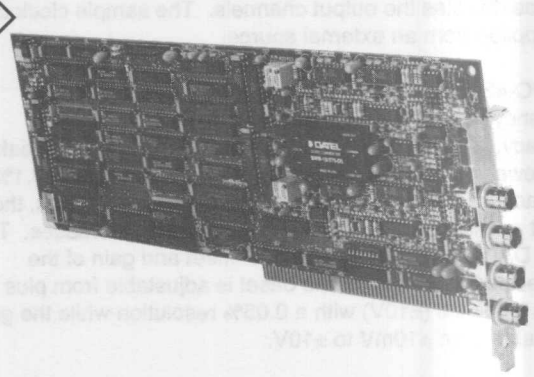
DATEL®
INNOVATION and EXCELLENCE

PC-420
Arbitrary Waveform Generator Board for IBM-PC/AT™ Computers

FEATURES

- **2 simultaneous analog outputs up to 10MHz**
- **Sample update rates to 40MHz**
- **High-resolution frequency synthesized clock**
- **Software programmable offset and gain**
- **8 software selectable low-pass filters per channel**
- **Stores up to 32k 12-bit waveform points per channel**
- **External clock, trigger, and gate inputs**
- **Waveform repetition up to 256 or continuously**
- **TTL level synchronization output**
- **Comprehensive Windows® graphic software with powerful equation resolver**

LabVIEW® Virtual Instrument!



GENERAL DESCRIPTION

The PC-420 is a high-speed, highly precise, arbitrary waveform generator board for IBM-PC/AT, PS-30, EISA bus and compatible computers. If your application requires simplicity without sacrificing performance, the PC-420 analog signal generator board offers two high-performance output channels for generating complex periodic and aperiodic analog signals simultaneously.

Unlike non-buffered analog output boards, the PC-420 combines versatility and programmability with high-resolution, variable gain and phase, local data buffering and software selectable filters to result in an effective, easy-to-use solution for waveform synthesis requirements. Using PC-420GEN waveform definition software, you can quickly produce any conceivable waveform.

The PC-420 uses digital synthesis to generate the analog output signals. Waveform pattern data for generating arbitrary functions (as well as sine, square, triangle and ramp outputs) is loaded from the host computer into waveform RAM on each channel. The waveform repeat depth is programmable from 2 to 32k samples and data scans can loop up to 256 times or forever. A fixed-frequency reference clock drives a Phase Locked Loop (PLL) to minimize phase jitter, transient response, and resolution problems inherent in earlier synthesizer designs.

Waveform sample points are clocked from the local buffers to a high-speed, 12-bit digital-to-analog converter stage at rates up to 40MHz. A stable internal 20MHz crystal oscillator ensures low output noise and controls waveform synthesis

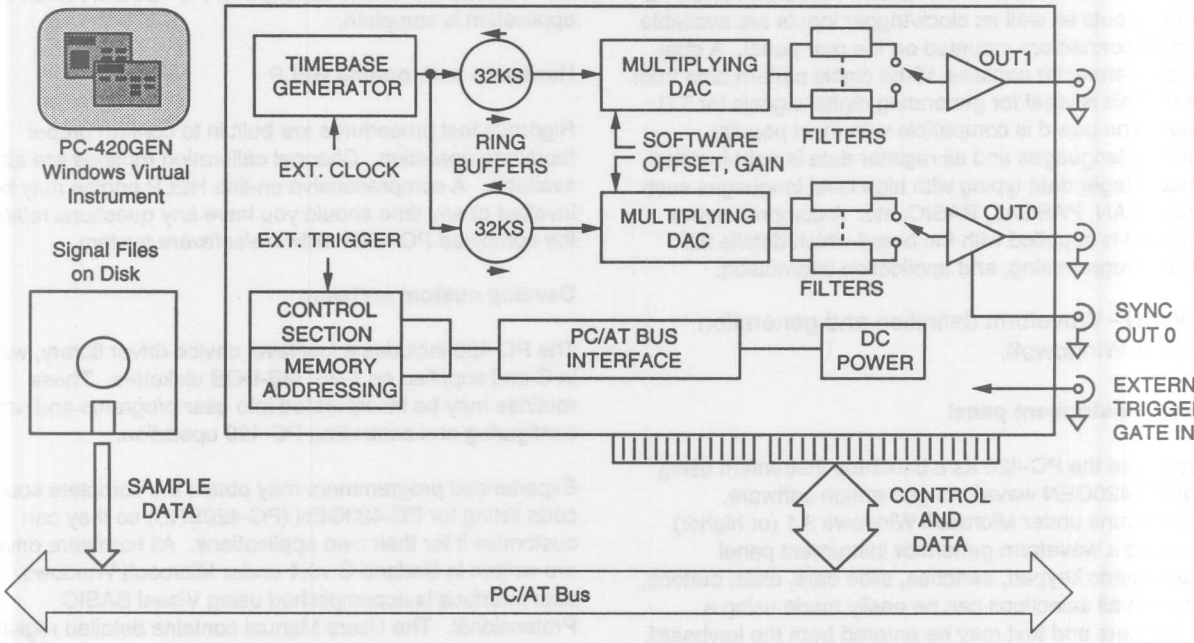


Figure 1. PC-420 Block Diagram

IBM-PC/AT is an IBM Corporation trademark.
Windows is a Microsoft Corporation trademark.
LabVIEW is a National Instruments trademark.

GENERAL DESCRIPTION (Continued)

by generating a 40MHz digitally synthesized sample clock source. An external trigger input synchronizes waveform scanning with your application. An external TTL "gate" input enables/disables the output channels. The sample clock can be supplied from an external source.

The PC-420 generates outputs at up to 10MHz with a frequency resolution of 0.012% and ±0.012% frequency accuracy. The signal amplitude range is 20V peak to peak for squarewaves. The resolution is 0.05% of full scale at 0.1% accuracy for sine wave outputs. For non-squarewaves, the output amplitude decreases as the frequency increases. Two 12-bit DAC's allow you to vary the offset and gain of the synthesized waveforms. The offset is adjustable from plus to minus full scale (±10V) with a 0.05% resolution while the gain is variable from ±10mV to ±10V.

Software selectable, fixed-frequency low pass anti-alias filters on each output channel ensure high spectral purity. Seven third order Butterworth low pass filters with a range of fixed cutoff frequencies from 10kHz to 10MHz (at the 3dB points), ensure proper waveform reconstruction and anti-aliasing and minimize harmonic distortion. In addition, each channel has a 20MHz low pass filter to eliminate high frequency system noise components from the output signals.

Software flexibility allows you to produce frequency, amplitude, phase, and burst modulated signals as well as linear and logarithmic frequency sweeps. Synthesized waveforms display the low phase noise and drift inherent to digital synthesis techniques. Wideband output amplifiers minimize distortion and exhibit excellent pulse response characteristics.

The PC-420 is configured on a full size PC/AT bus card that is fully contained within the host computer. Waveform and TTL level sync outputs as well as clock/trigger inputs are available on four BNC connectors mounted on the rear panel. A dual row, header connector contains 16-bit digital pattern data from channel 0. This is ideal for generating digital signals for TTL circuit test. The board is compatible with most popular programming languages and all register data is right-justified to facilitate integer data typing with high level languages such as C, FORTRAN, PASCAL, BASIC, etc. A comprehensive Users Manual is supplied with the board which details full installation, programming, and application information.

PC-420GEN - Waveform definition and generation software for Windows®.

Easy to use instrument panel

It is easy to use the PC-420 as a benchtop instrument using DATEL's PC-420GEN waveform generation software. PC-420GEN runs under Microsoft Windows 3.1 (or higher) and simulates a waveform generator instrument panel including numeric keypad, switches, slide bars, dials, buttons, etc. Although all selections can be easily made using a mouse, numbers and text may be entered from the keyboard. It is simple to use and requires *no* low level programming by the user. A TTL level "sync" output indicates 0V crossing on channel 0 - allowing you to phase synchronize scanning with your external hardware.

Select or create any waveform

You can select from a repertoire of standard sine, cosine, square, triangle and sawtooth waves. You can generate noise and add it to the waveform - ideal for communications circuit testing and determining the performance bounds of a system.

Equation resolver, disk files

A powerful equation parser allows high speed formulation of any complex mathematical function. Upload previously created data files for regeneration by the PC-420. Waveforms may be displayed on screen before scanning and also during wave generation. The present hardware configuration can be viewed, edited, and saved to a data file for use later.

Generate waveform

Select the clock and trigger sources. Specify the frequency, amplitude, offset, and phase of the output signals. Choose from one of seven reconstruction filters for each of the two output channels. Start waveform generation on a single output channel or on both channels simultaneously.

Multitasking

After creating a waveform and configuring the hardware you may *Close* the instrument panel screens and execute other applications software in the Windows environment. The predefined waveforms continue to be generated at each output channel by the PC-420, i.e. PC-420GEN continues to execute in the background. This is ideal for running long, dynamic test sequences while the host computer concurrently carries out other tasks. Simply *Exit* PC-420GEN when the application is complete.

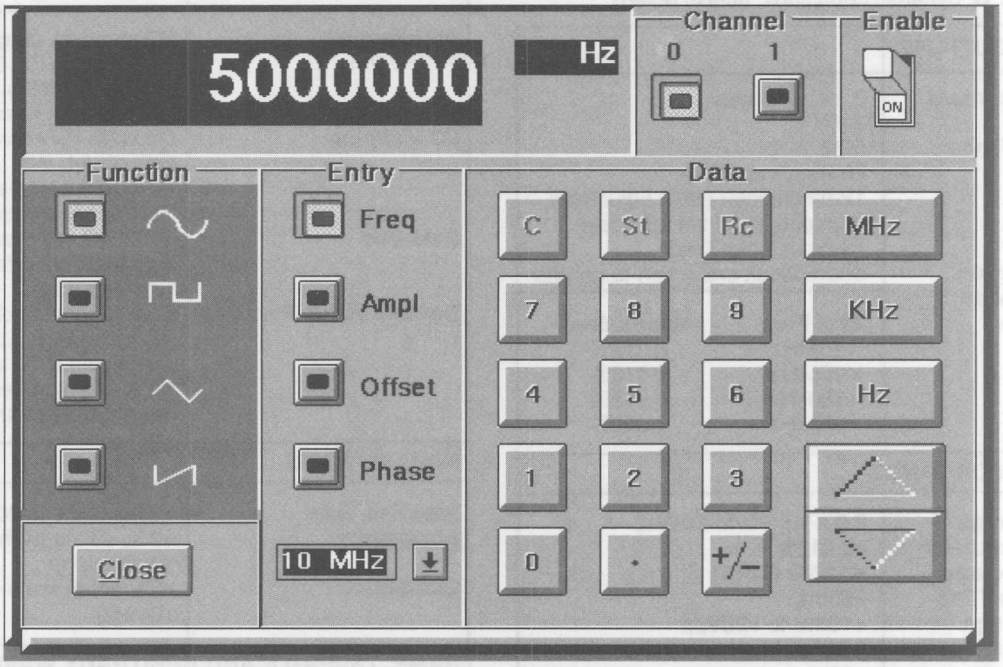
Hardware test, on-line HELP

Rigorous test procedures are built in to confirm proper hardware operation. Channel calibration routines are also available. A comprehensive on-line HELP engine may be invoked at any time should you have any questions related to the combined PC-420 hardware/software system.

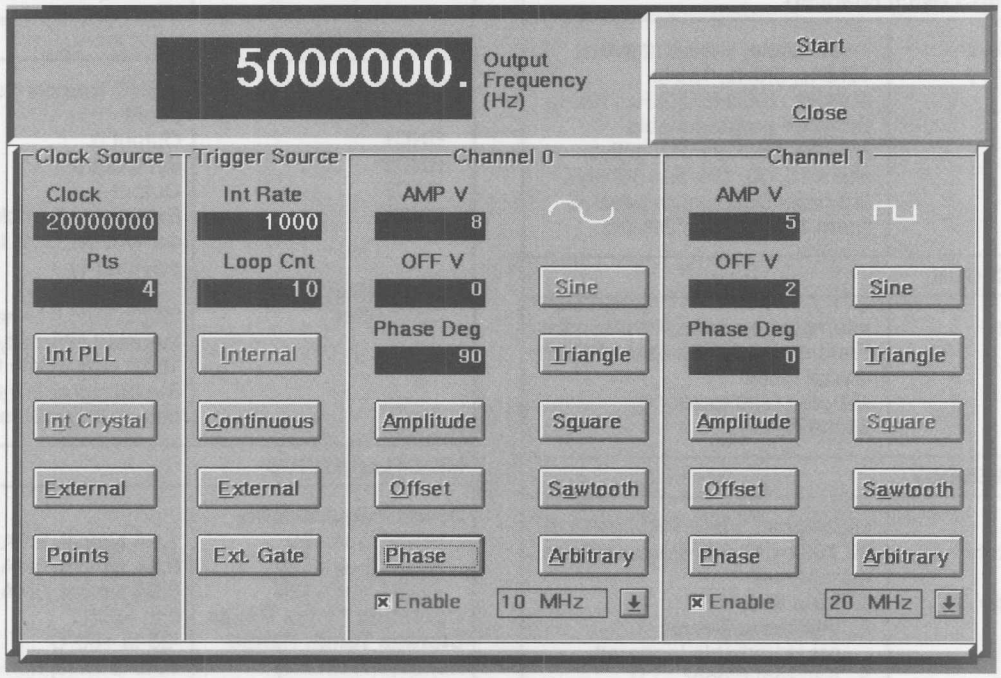
Develop custom software

The PC-420 includes a low-level device driver library, written in C and supplied on 5.25" MS-DOS diskettes. These routines may be incorporated into user programs and used for configuring and controlling PC-420 operation.

Experienced programmers may obtain the complete source code listing for PC-420GEN (PC-420SRC) so they can customize it for their own applications. All hardware drivers are written in Borland C v3.1 under Microsoft Windows. The user interface is accomplished using Visual BASIC Professional. The Users Manual contains detailed register and timing information as well as example software routines to help users develop their own code.



PC-420GEN Standard Waveform Panel. Select a sine, square, triangle, or sawtooth wave; specify frequency amplitude, offset and phase of the signal. Enter all data at the keypad as though it were a real instrument. Specify the reconstruction filter for each channel and turn the instrument *ON* to generate the waveform. *Close* when done, and the generated signals remain on the output channels.



PC-420GEN Arbitrary Waveform Panel. Select the clock source, trigger sources and sample scan loop count. Enter the arbitrary waveform file name, load it into PC-420 waveform RAM. Specify amplitude, offset, and phase of each output waveform. Select filter and start single or dual channel scanning. *Close* when done, and the generated signals remain on the output channels.

FUNCTIONAL SPECIFICATIONS
(Typical at +25°C, dynamic conditions, unless noted)

WAVEFORM OUTPUTS	
Number of Channels	2, non-isolated
Amplitude	±10V
Output Impedance	50Ω
Update Rate	40MHz, maximum
Offset Adjust	12-bit unipolar DAC, adjustable from plus to minus full scale
Gain Adjust	12-bit unipolar DAC
Output Protection	Short circuit protection to ground
Output Bandwidth	

Waveform	Max Freq.	Resolution
Sine	10MHz	0.012%
Square	10MHz	0.012%
Ramp	100kHz	0.012%
Triangle	100kHz	0.012%

OUTPUT PERFORMANCE	
Frequency Range	2.3 x 10^{-3}Hz to 10MHz
Frequency Accuracy	±0.012%
Amplitude Accuracy	±0.25% of FSR
Loop Lock Up Time	250ms
Amplitude Range	+10mV to +20Vpp
Amplitude Resolution	0.05% of full scale (12-bit DAC)
Maximum Offset	±10V
Offset Resolution	0.05% of full scale
Sync. Output	TTL levels into 50Ω, on channel 0 only, active high
TTL Output Rise/Fall Time	5 nanoseconds
Gain/Offset DAC Settling Time	15 microseconds

ANALOG FILTERS (each channel)	
Number of Filters	7 selectable, 1 fixed (20MHz)
Cutoff Frequency (-3db down)	10MHz, 5MHz, 1MHz 500kHz, 100kHz, 50kHz, 10kHz
Selection	Software programmable
Filter Type	3rd order Butterworth active filters 10, 50, 100 and 500kHz. 3rd order Butterworth passive filters 1, 5, 10, and 20MHz.

WAVEFORM CLOCK	
Clock Sources	Internal or external, 40MHz max.
Internal Clock	Frequency synthesizer or 20MHz crystal clock
Accuracy	±50ppm (+20 to +30°C)
Aging	±5ppm/year

WAVEFORM MEMORY	
Architecture	High-speed, static RAM (SRAM)
Memory Capacity	32,768k x 16 waveform samples per channel
Operating mode	1. Free run 2. Internal software programmable triggered 3. External trigger - TTL 4. External gate - TTL

PC/AT BUS INTERFACE	
Architecture	I/O mapped, pluggable to IBM-PC/AT, PS-30, EISA bus and compatibles. Decodes eight 16-bit I/O registers.
I/O Mapping	Decodes I/O address lines A9 through A4. A3. . .A0 are decoded for individual register access. Highest base address is 3F0 hex.
Data Bus	16-bit I/O transfers; all data is right justified, offset binary, sign-extended.
Control/Status Function	Board reset, clock and trigger select, timer control, filter select, offset/gain DAC loading, frequency synthesizer control, memory select and load.

SQUARE WAVE	
Rise/Fall Time	<10ns (10% to 90%)
Asymmetry	<2%, ±30ns (with 50Ω termination)
Overshoot	<5% at full scale output (to 10MHz)

RAMP, TRIANGLE AND ARBITRARY WAVEFORMS	
Rise/Fall Time	40ns with 50Ω termination
Linearity	±0.1% of full scale output

ARBITRARY WAVEFORMS	
Sample Rate	40MHz
Waveform Length	4 to 32,768 points
Vertical Resolution	12 bits (0.025% of full scale)

CONNECTORS	
Signal Connectors	4 BNC type connectors on rear panel
BNC1	Output 0
BNC2	Sync out 0
BNC3	Output 1
BNC4	External trigger/clock inputs (TTL compatible, 50Ω terminal, jumper selectable)
Digital Pattern Connector	26-pin dual-row header connector mounted internally. Contains 16-bit digital data from channel 0. Strobe signal included for clocking data to external receivers.

MISCELLANEOUS	
Power Requirements	
PC/AT bus +5V	1.6A typical, 2.0A maximum
PC/AT bus +12V	0.3A typical, 0.4A maximum
PC/AT bus –12V	0.3A typical, 0.4A maximum
Operating Temp. Range	0 to +60°C
Storage Temp. Range	-25 to +80°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet (0 to 3047m)
Outline Dimensions	4.5"H x 13.31"L x 0.5"W (11.43 x 33.81 x 1.59cm), Full size PC/AT board. Uses a single PC/AT slot.
Weight	14oz. (0.42kg)

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PC-420 FREQUENCY DOMAIN PERFORMANCE (Typical)

Note: Readings are based on visual interpretation of a graphic FFT display. Results will vary depending on FFT algorithm, screen resolution, and spectrum analyzer performance.

Table 1. Frequency Response - No External Filter

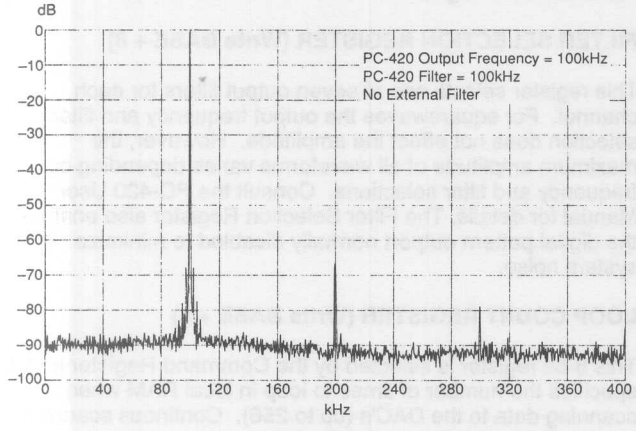
PC-420 Output Frequency	PC-420 Filter Frequency	Noise Floor	2nd Harmonic	3rd Harmonic
10kHz	10kHz	-90dB	-75dB	-83dB
50kHz	50kHz	-80dB	-72dB	-78dB
100kHz	100kHz	-90dB	-66dB	-73dB
500kHz	500kHz	-85dB	-60dB	-70dB
1MHz	1MHz	-83dB	-55dB	-69dB
5MHz*	5MHz	-80dB	-50dB	-58dB
10MHz*	10MHz	-80dB	-45dB	-54dB

Note: Load impedance = 1MΩ, internal filter enabled
* Load impedance = 50Ω, internal filter enabled

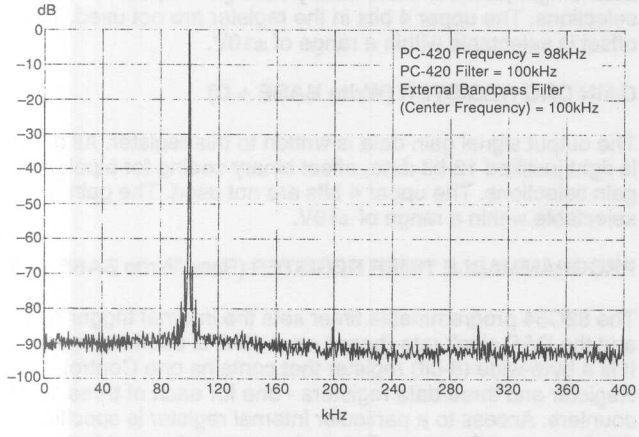
Table 2. Frequency Response - External Bandpass Filter Frequency = PC-420 Output Frequency

PC-420 Output Frequency	PC-420 Filter Frequency	Noise Floor	2nd Harmonic	3rd Harmonic
98kHz	100kHz	-90dB	-85dB	-83dB
480kHz	500kHz	-88dB	-88dB	-85dB
975kHz	1MHz	-88dB	-82dB	-80dB
2.45MHz	5MHz	-83dB	-82dB	-80dB

Note: Load impedance = 50Ω, internal filter enabled.



No external filter



External bandpass filter
(center frequency = 100kHz)

Figure 2. PC-420 FFT Plots (sinewave inputs)

OUTPUT AMPLITUDE CONSIDERATIONS

Table 3. Output Amplitude vs. Filter Selection

Output Frequency Filter Frequency	Amplitude (without filter)	Amplitude (with filter)
10kHz	±10V	±7V
50kHz	±10V	±7V
100kHz	±10V	±7V
500kHz	±10V	±7V
1MHz	±10V	±7V
5MHz	N/A	±5V
10MHz	N/A	±5V

All readings taken into a 1MΩ load with the 20MHz fixed internal filter. If a 50Ω load is connected the output amplitudes will attenuate by half.

For signal frequencies up to 1MHz the output amplitude depends on the filter cutoff frequency. Table 3 reflects the output levels when the filter frequency equals the signal frequency, i.e. the full scale amplitude (±10V) is decreased by 3dB. Selecting a filter frequency higher than the output frequency will result in less attenuation but signal reconstruction quality will suffer. Above 1MHz the output amplifier's finite bandwidth also attenuates the output signal.

Conclusion: Waveform amplitude and signal quality depends on output frequency **and** filter selection.

I/O REGISTER MAP

(Refer to the PC-420 User's Manual for detailed programming information and register bit fields.)

The PC-420 appears to the host computer as a set of I/O registers. The BASE address is switch selectable and can be located anywhere up to 3F0 hex on 16-byte boundaries. This allows installing multiple boards in the same host at the same time. Each individual I/O register is located at a fixed offset from this BASE as shown in Table 4.

Table 4. PC-420 I/O Register Map

I/O Address (hex)	Direction	Description
BASE + 0	Write	Command Register
BASE + 0	Read	Status Register
BASE + 2	Write	Start Address Register
BASE + 2	Write	Final Address Register
BASE + 4	Write/read	Memory Data Register
BASE + 6	Write	Frequency Synthesizer Register
BASE + 8	Write	Filter Selection Register
BASE + 8	Write	Loop Count Register
BASE + A	Write/read	Offset DAC Register
BASE + C	Write/read	Gain DAC Register
BASE + E	Write/read	Programmable Timer Register

At power up or PC bus reset, both output channels are set to 0V. All register data is right justified and 16-bit I/O word instructions must be used to access each register. The registers may be programmed in any sequence as long as the Command Register bits that enable the outputs are written last.

REGISTER DESCRIPTIONS

COMMAND REGISTER (Write BASE + 0)

This is a 16-bit wide register that controls PC-420 programming and controls operation. It allows host software to specify other local hardware registers for programming or for reading status information. These include the filter register selection, offset and gain DAC selection, 82C54 timer, and memory register selections. It also specifies the clock and trigger sources, i.e., internal or external. When ready to start generating waveforms from local RAM, the Command Register enables the output channels - individually or simultaneously.

STATUS REGISTER (Read BASE + 0)

The Status Register resides at the same I/O address location as the Command Register but it displays a different bit representation. It is read only and it reports the output channel level (with respect to 0V) and echoes the status of the phase locked loop section.

START ADDRESS REGISTER (Write BASE + 2)

This register must be loaded with the start address in waveform RAM for a data scan. It also doubles as the present RAM address when loading signal files from disk. It is selected by the Command Register. Local hardware on the PC-420 compares the start (present) and final register contents during a scan and restarts the waveform scan when equal. The loop count is programmable up to 256 by writing the Loop Count Register at BASE + 8. Continuous mode is selected in the Command Register.

FINAL ADDRESS REGISTER (Write BASE + 2)

This is selected by the Command Register. It contains the final RAM address when scanning data to the output DAC's. When the present address is equal to this final address, the local memory pointer circulates back to the start address and the scan repeats. The number of times is specified in the Loop Count. Continuous mode is selected in the Command Register

MEMORY DATA REGISTER (Read/Write BASE + 4)

12 bit waveform data is loaded to local PC-420 RAM through this register. The address is placed using the Start Address Register as a current address. The memory bank being accessed is selected by the Command Register. All data is right justified, raw binary data with offset binary coding to allow for bipolar output waveforms.

FREQUENCY SYNTHESIZER REGISTER (Write BASE + 6)

Data for programming the frequency systhesizer counters is written to the lower 4 bits of this register. The upper 12 bits are not used. Individual counters are selected for access in the Command Register.

FILTER SELECTION REGISTER (Write BASE + 8)

This register selects one of seven output filters for each channel. For squarewaves the output frequency and filter selection does not effect the amplitude. However, the maximum amplitude of all waveforms varies depending on frequency and filter selections. Consult the PC-420 User Manual for details. The Filter Selection Register also enables the digital pattern outport normally disabled to minimize system noise.

LOOP COUNT REGISTER (Write BASE + 8)

This 8-bit register is selected by the Command Register and it specifies the number of times to loop in local RAM when scanning data to the DAC's (up to 256). Continous scanning is selected by the Command Register.

OFFSET DAC REGISTER (Write BASE + A)

This 12 bit write only register sets the output signal offset. All data is right justified, offset binary coding for bipolar selections. The upper 4 bits in the register are not used. The offset is selectable within a range of ±10V.

GAIN DAC REGISTER (Write BASE + C)

The output signal gain data is written to this register. All data is right justified 12-bit data, offset binary coding for bipolar gain selections. The upper 4 bits are not used. The gain is selectable within a range of ±10V.

PROGRAMMABLE TIMER REGISTER (Read/Write BASE + E)

The 82C54 programmable timer sets the internal trigger rate and the DAC clock rate (based on a 10MHz oscillator input). It is a byte-wide (8-bit) register that contains one Control Register and three data registers - one for each of three 16-bit counters. Access to a particular internal register is specified in the Command Register. Detailed programming and timing information is available in the PC-420 User's Manual.

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PROGRAMMING SEQUENCE

PC-420GEN provides all the waveform creation, upload, and generation facilities without any low level programming by the user. However, custom applications may require some software development - either modification of PC-420SRC or complete hardware coding. The low level driver library supplied with PC-420 will be very helpful when writing code.

The following flow diagram illustrates PC-420 programming strategy. Complete programming details and example code listings are in the PC-420 User's Manual.

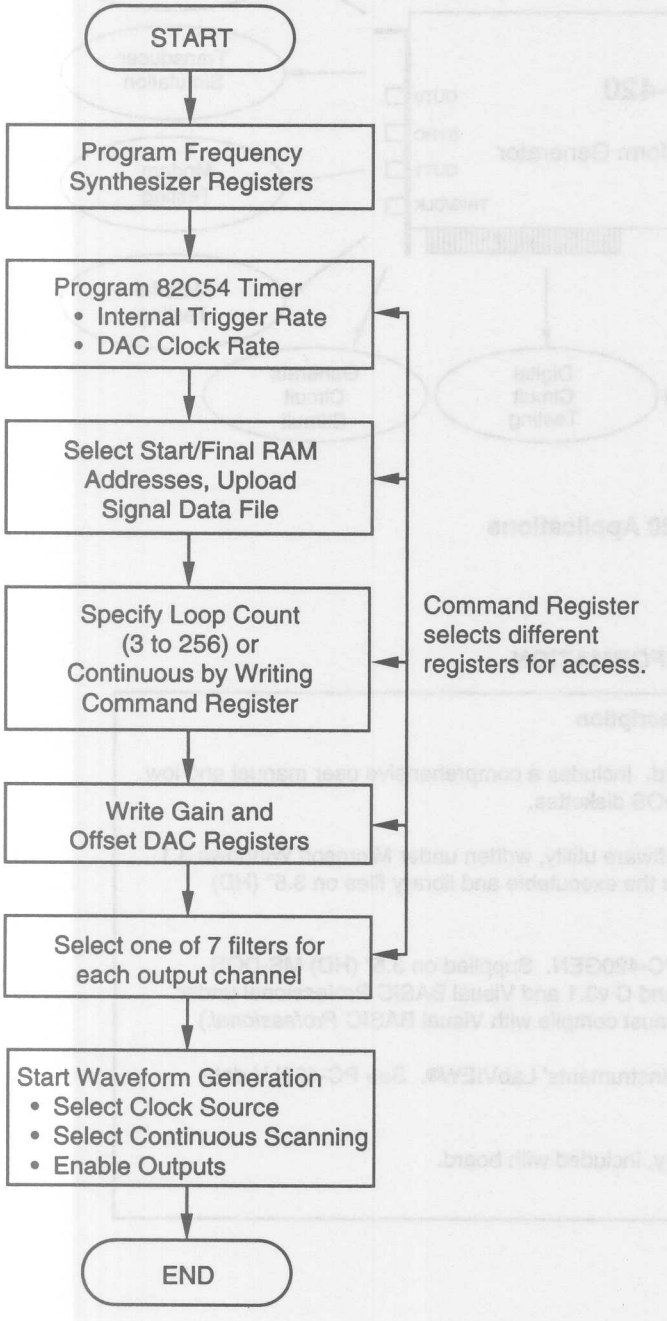


Figure 2. PC-420 Programming Flow Chart

Note: Waveform data must be uploaded from disk file to PC-420 RAM **before** starting generation. Data cannot be uploaded from disk while DAC's are clocking.

SIGNAL DATA FILES

Waveform data must be loaded from disk file to local RAM on each PC-420 channel **before** scanning. All data must be 12 bits wide, right justified raw binary data with offset binary coding to allow for bipolar output ranges. It may be created mathematically by host software or generated by an A/D board e.g., DATEL's PC-414 fast analog input board.

The file can be uploaded to the PC-420 RAM using most high level programming languages that can do I/O accesses, e.g. "C", BASIC, FORTRAN, etc. This is done through the Memory Data Register at BASE + 4. Individual addresses are specified in the Start Address Register at BASE + 0Ah. No hardware configuration header information can be included unless host software strips it from the signal data before loading. Scan modes and scan rates can be programmed directly by host software.

Note: PC-420GEN contains a powerful equation parser that will resolve and evaluate any complex waveform equation entered by the user. The parser will then generate the appropriate data file. PC-420GEN uploads this data file to local waveform RAM and generates the desired waveform. A waveform plotting utility in PC-420GEN allows you to confirm proper signals before scanning.

The PC-420 waveform RAM repeat depth is programmable from 4 to 32,768 samples by setting the Start and Final memory addresses. Data scanning can loop on this up to 256 times or continuously - a non-stop "forever" mode. The loop count is programmable via the Loop Count Register at BASE + 8. Continuous mode is selected in the Command Register.

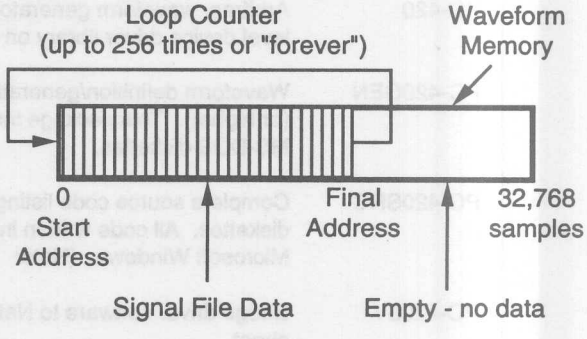


Figure 3. PC-420 Waveform Buffer Scanning

One period of a waveform only needs to be loaded to PC-420 RAM. By looping on this, a continuous waveform may be generated. Be aware that concatenated data files and truncated waveforms can be discontinuous at their boundaries - resulting in glitches in the output signals. A graphic waveform editor is the ideal solution to smoothing such files *before* loading them to the PC-420.

APPLICATIONS

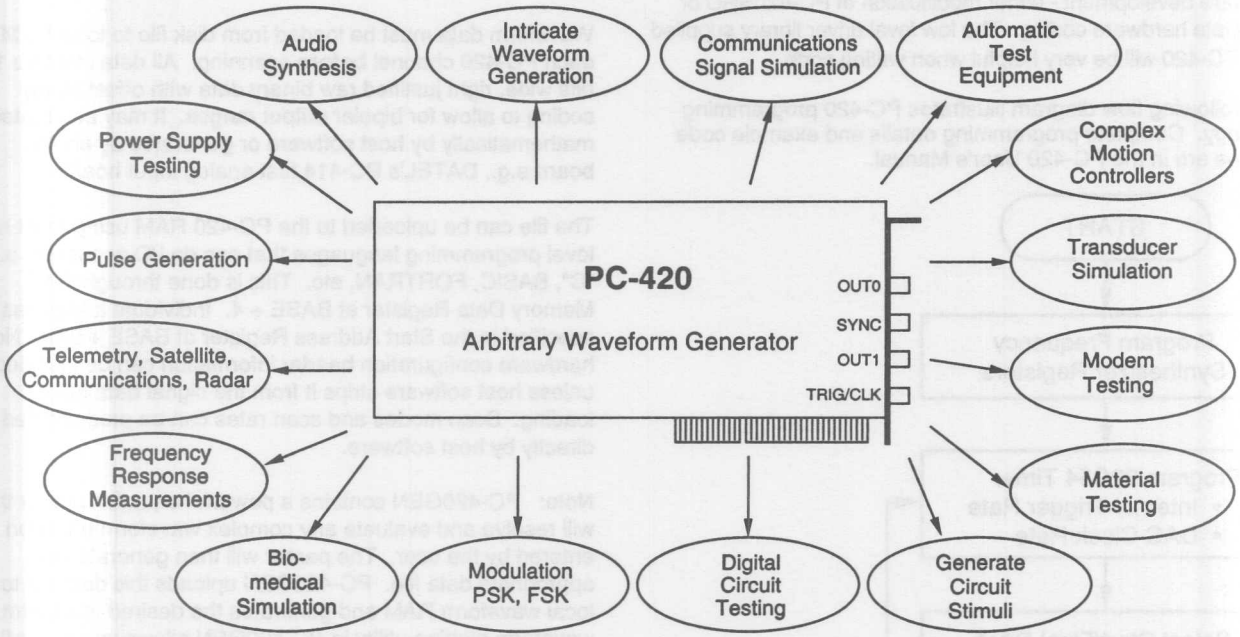


Figure 4. PC-420 Applications

ORDERING INFORMATION

Model	Description
PC-420	Arbitrary waveform generator board. Includes a comprehensive user manual and low level device driver library on MS-DOS diskettes.
PC-420GEN	Waveform definition/generation software utility, written under Microsoft Windows 3.1 (or higher). This package includes the executable and library files on 3.5" (HD) MS-DOS diskettes.
PC-420SRC	Complete source code listing for PC-420GEN. Supplied on 3.5" (HD) MS-DOS diskettes. All code written in Borland C v3.1 and Visual BASIC Professional under Microsoft Windows. (Note: You must compile with Visual BASIC *Professional*.)
PC-420LV	Bridge driver software to National Instruments' LabVIEW®. See PC-420LV data sheet.
PC-420DRV	Low level source code driver library, included with board.

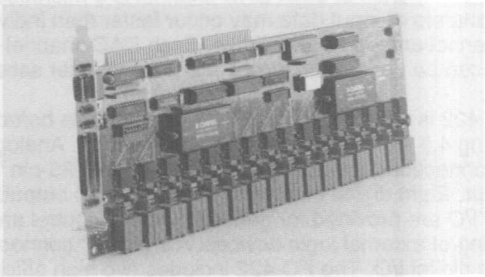
DATEL®
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PC-422
Fast, Simultaneous, 16-Channel PC/AT Analog Output Board

FEATURES

- **8 or 16 analog outputs**
- **12-bit D/A resolution**
- **3 microsecond settling time**
- **Simultaneous update**
- **Trigger timer interrupt**
- **Digital I/O (4-in, 4-out)**
- **Output ranges selectable per channel**

LabVIEW® Virtual Instrument!



DESCRIPTION

Many applications require phase-synchronous analog outputs. Examples include precision system simulation and coherent field generation in process control, audio, acoustics and sonar. The PC-422 is a high density analog output board with up to 16 signal channels. Each digital to analog Converter (DAC) channel may be individually selected for full scale output ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, or ±10V. All outputs are buffered and will deliver ±0.025% accuracy from 0 to 5 milliamps output load. The PC-422 is installed in a host IBM-PC/AT or compatible computer.

To achieve the simultaneous update capability, each channel input register is double buffered. The registers are successively loaded by the host computer then all channels are updated by host command or trigger. If preferred, each channel may also be operated in the non-concurrent transparent mode under program control with random addressing or single channel operation.

For applications requiring a precision clock to sequence the output waveforms, the PC-422 includes a software-programmable trigger. The trigger strobes the simultaneous update and posts a status bit or interrupt to the host PC. Upon detecting the trigger, the host may block-load the next data frame. The trigger may be derived from an internal crystal-stabilized timer or from an external timer base. The external trigger option makes the PC-422 fully synchronous with external events. The trigger section includes a spare output counter, usable for any purpose.

For repeating frame scan applications, the PC-422 includes an auto-increment mode. In this mode, block transfer I/O string instructions will automatically load up to 16 channels at very high speed from a memory buffer in the PC. The PC-422 will digitally steer each analog data word to successive DAC input registers while using the same I/O data register address. The user's program simply maintains the 80X86 CX register as a downcounter to terminate each block transfer. Typically, the trigger and auto-increment modes are used together where the PC loads the next block after detecting the trigger status signal from the last simultaneous update.

The combination of a precision frame clock trigger, auto-increment channel addressing and high speed simultaneous block loading make the PC-422 ideal for artificial waveform applications. Such waveform generators continuously loop through a large RAM buffer containing a synthetic composite digitized analog signal.

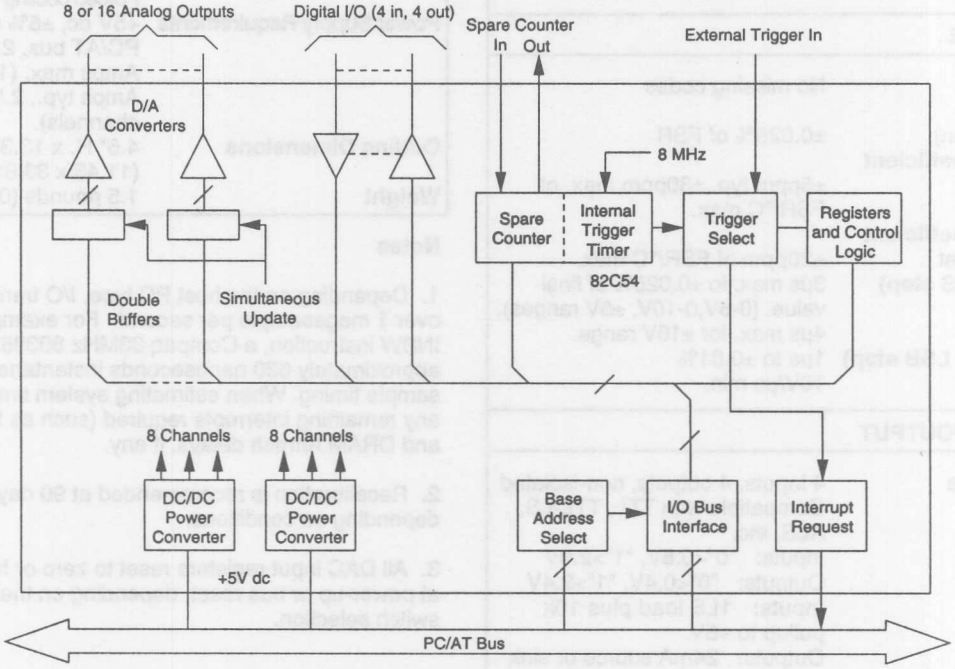


Figure 1. PC-422 Block Diagram

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LabVIEW is a National Instruments trademark

GENERAL DESCRIPTION CONT.

Fast settling rates are another feature of the PC-422. Full scale step response of each DAC channel is 3 microseconds. Block transfers of input data may occur faster than individual DAC channel analog settling times. Each DAC channel input register can be updated at over 1 Megasample per second.

The PC-422 is configured on a PC/AT compatible board measuring 4.5 inches high by 13.31 inches long. Analog signal connections are made using a rear panel 25-pin "D" connector. Eight digital channels (4 inputs and 4 outputs) of discrete I/O are provided for general purpose control and monitoring of external logic devices. A 9-pin "D" connector provides digital I/O. The PC-422 includes two high efficiency DC to DC power converters to supply local analog circuits. The entire board uses only +5 Volt DC power from the PC/AT bus. The board is compatible with all popular computer languages although the highest speed will require assembly language. A comprehensive user's manual is included with the board showing full programming and application information.

SPECIFICATIONS

(typical at +25°C, dynamic conditions, unless noted)

ANALOG OUTPUTS	
Number of Channels	8 or 16
Output Configuration	single-ended, non-isolated
Full Scale Output Ranges	0 to +5V, 0 to +10V, ±2.5V, ±5V, ±10V, individually selectable per channel.
Output Current	0 to ±5 mA min. (source or sink), short-circuit protected to ground.
Resolution	12 binary bits.
Input Data Coding	Straight or offset binary, positive true coding. Data is right justified. See note 3.
Output Impedance	50 milliohms
Channel Addressing Modes	Random, simultaneous or auto-increment sequential.

PERFORMANCE	
Monotonicity	No missing codes
Linearity Error (after calibration)	±0.025% of FSR
Temperature Coefficient of Gain	±5ppm typ.,±30ppm max. of FSR/°C max.
Temperature Coefficient of Zero or Offset	±20ppm of FSR/°C max.
Settling Time (FS step)	3µs max. to ±0.025% of final value. (0-5V,0-10V, ±5V ranges). 4µs max. for ±10V range.
Settling Time (1 LSB step)	1µs to ±0.01%
Slew Rate	10V/µs min.

DIGITAL INPUT/OUTPUT	
Number of Lines	4 inputs, 4 outputs, non-isolated
Logic Levels	Compatible with TTL, TTL-LS, ALS, etc. Inputs: "0"<0.8V, "1">2.0V Outputs: "0"<0.4V, "1">2.4V
I/O Loading	Inputs: 1LS load plus 10k pullup to +5V. Outputs: 24mA source or sink

COUNTER/TIMER	
Function	Used as an update strobe for each multichannel DAC frame.
Frequency Range	4MHz to 1073.77 seconds (32-stage binary or BCD divider).
Frequency Stability	±50ppm/°C
Spare Counter	16-stage binary divider usable for any purpose. Will divide input signals from 1 to 65,536. Includes counter input and output, 1 TTL-LS load, 10MHz max input.

PC/AT BUS INTERFACE	
Architecture	I/O mapped in 8 contiguous word locations on 16-byte boundaries.
I/O Mapping	Decodes I/O address lines A9 through A4. Maximum base address is 3F0h.
Data Bus	16-bit I/O transfer.
Trigger Interrupt	1 interrupt, software-selectable on level 7, 9, 10, 11 or 15.

MISCELLANEOUS	
Analog Section Adjustments	Full scale gain and zero or offset potentiometers are provided for each DAC channel. See note 2.
Analog Connector [P1]	25-pin DB-25S, also includes the external trigger input.
Digital I/O Connector [P2]	9-pin DB-9S
Spare Timer/Counter	On-board header pins
Operating Temp Range	0 to +60°C
Storage Temp Range	-25 to +85°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet (0-3048 m). Forced cooling is recommended.
Power Supply Requirements	+5V dc, ±5% supplied from PC/AT bus. 2.5 Amps typ., 4.0 Amps max. (16 channels), 1.5 Amps typ., 2.5 Amps max. (8 channels).
Outline Dimensions	4.5" H. x 13.31" L x 0.5" W (11,43 x 33,81 x 1,27 cm)
Weight	1.5 pounds (0,7kg)

Notes

1. Depending on the host PC type, I/O transfers may occur over 1 megasample per second. For example, using the REP INSW instruction, a Compaq 33MHz 80386 host achieved approximately 630 nanoseconds instantaneous sample to sample timing. When estimating system timing, account for any remaining interrupts required (such as the real time clock) and DRAM refresh delays, if any.

2. Recalibration is recommended at 90 day intervals, depending on conditions.

3. All DAC input registers reset to zero or half-scale (0800h) at power-up or bus reset, depending on the unipolar/bipolar switch selection.

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PROGRAMMING NOTES

There are three ways to cause an update of the DAC registers. Either a register write may be used, or the internal trigger clock or an external digital trigger input.

To load multiple scans from a large host memory array, use the following sequence:

Program the channel address register for the starting address. Program the command register for auto-increment and trigger updating. Load the first scan into the data channels. Your load program will have to count the number of loads then exit.

1. Poll the status register to detect the trigger. If the trigger was not received, continue polling.

2. When the trigger occurs, optionally test the overrun flag and report any errors. To save time, overrun testing may be deleted if you are sure no data was lost.

3. When the trigger occurs, block load the next data scan while advancing the PC's buffer memory address pointer. For the highest speed, use the 80X86 CX register or other index as a downcounter to terminate the load. Also, if this is a circular host buffer, remember to wrap the pointer to the bottom of the buffer when it reaches the top.

4. If the DAC channel address did not wrap around exactly to channel zero, write the new start channel address.

5. Write to the simultaneous update register to arm the trigger update ready flag.

6. If more scans are needed, go to step 1.

Trigger status polling should be used for the very highest speed. If somewhat lower update rates are needed, DAC refresh may use either the trigger interrupt or by polling. The trigger interrupt is especially useful if other system tasks are concurrent, such as disk I/O or graphics screen writes.

I/O REGISTER MAPPING

The base address may be selected anywhere up to 3F0h on 16-byte boundaries. At power-up or PC bus reset, all control registers contain zeroes. The DAC data register should be programmed after setting up the channel address and command mode. The 82C54 registers must be programmed in a specific sequence, discussed in the user manual. 16-bit I/O word instructions must be used. Unlisted registers are not used.

I/O Address (hex)	Direction	Description
BASE + 0	Write	Command Register
BASE + 0	Read	Status Register
BASE + 2	Write	DAC Channel Address Register
BASE + 4	Write	DAC Data Register
BASE + 6	Write	Simultaneous Update Register
BASE + 8	Read/Write	Counter 0 (82C54)
BASE + 0Ah	Read/Write	Counter 1 (82C54)
BASE + 0Ch	Read/Write	Counter 2 (82C54)
BASE + 0Eh	Read/Write	Control Word Register (82C54)

Note: "x" bits are "don't care".

COMMAND REGISTER (Write I/O BASE + 0)

15 - 11	10 9 8	7	6	5	4	3 2 1 0
Not Used	Intrpt Level 2 1 0	Simul Updt Sel	Simul Updt Mode	Ext/ Int Trig	Chan Auto Incr	Digital Outport 3 2 1 0

Digital Outport [Bits 3, 2, 1, 0] — Discrete digital outputs are written to these bits.

Channel Address Auto-increment [Bit 4]
0 = No channel increment
1 = Increment channel address after a DAC data register write.

In the non-increment mode (bit 4 = 0), successive writes to the DAC data register will load into a single DAC channel selected by the last address written into the channel address register.

In auto-increment mode (bit 4 = 1), the channel address will advance after each data register write. The address will cycle around to channel 0 after reaching channel 15, modulo 16.

Trigger Source Select [Bit 5]
0 = Internal trigger
1 = External trigger

The trigger may be supplied either from the internal clock (counters 0 and 1) or from an external digital trigger input. In the update mode (bit 6 = 1, bit 7 = 1), the trigger strobes all DAC channels simultaneously from previously written DAC data.

Simultaneous Update Mode [Bit 6]
0 = Update via the simultaneous update register (Write BASE + 6).
1 = Update via internal or external trigger.

Simultaneous update causes all 8 or 16 DAC channels to be loaded with data that was last written to their input registers. If command bit 6 = 0, the trigger will be inhibited.

Simultaneous Update Select [Bit 7]
0 = Transparent mode (immediate DAC conversion of input data)
1 = Hold data until update.

With bit 7 = 0, DAC analog outputs will follow their input data values as fast as those values are written. If bit 7 = 1, updating the DAC outputs will wait until the trigger or a write to the update register.

Interrupt Level Select

Bit 10	9	8	
0	0	0	= No interrupt
0	0	1	= Interrupt Request Level 7
0	1	0	= Interrupt Request Level 9
0	1	1	= Interrupt Request Level 10
1	0	0	= Interrupt Request Level 11
1	0	1	= Interrupt Request Level 15
1	1	0	= No interrupt
1	1	1	= No interrupt

These bits bits select the IRQ line on the PC/AT bus where trigger interrupts are placed.

STATUS REGISTER (Read I/O BASE + 0)

15	14	13 12	11 - 8
Update Ready Status	Over Run Error	Not Used x x	Current Channel Address 3 2 1 0

7	6	5	4	3 2 1 0
Simul. Update Select	Simul. Update Mode	External/ Internal Trigger	ChanAddrs Auto Increment	Digital Inport 3 2 1 0

Bits 4-11 may be used to verify bits loaded into the command register.

Digital Inport [Bits 3, 2, 1, 0] — Discrete digital inputs may be read in these bits.

Status Bits [Bits 7-4] — These bits follow the corresponding bits in the command register.

Current Channel Address [Bits 11-8] — These bits indicate either the last address written into the channel address register or the next channel address to be written to by the next DAC data write.

These addresses will sequence from channel 0 to 15, modulo 16 in auto-increment mode.

Overrun Error [Bit 14] — In trigger update mode (command 6 = 1) this bit will be set to one if a trigger occurs before the next load of the DAC data register. Any write to the command register resets bit 14 to zero.

Update Ready Status [Bit 15] — With command bit 7 = 1, a write to the simultaneous update register will set bit 15 to one. The trigger will reset this bit to 0, indicating that the next frame of data may be loaded. If a trigger occurs before bit 15 is set to 1, the overrun error bit will be set to 1.

Bit 15 is normally polled to detect the trigger after loading the data registers. Bit 15 stays at 0 if command bit 6 = 0.

ORDERING GUIDE

Model	Number of channels
PC-422A	8
PC-422B	16

Boards are fully tested and include a manual.

PC-422SET Setup and configuration program on 3.5-inch MS-DOS disks. Provides calibration and test waveforms.
PC-422SRC Source code to PC-422SET
PC-422LV Bridge driver software to National Instruments' LabVIEW. See PC-422LV data sheet.

CHANNEL ADDRESS REGISTER (Write I/O BASE + 2)

15 - 4	3 2 1 0
Not Used	Channel Address 3 2 1 0

In non-auto-increment mode, these bits select the address of the next channel to be written to by the DAC data register. The address must be selected before writing data to a channel.

In auto-increment mode, these bits determine the starting channel address. After each data register load, addressing is automatically sequenced. The addressing cycles around to channel 0 after reaching channel 15.

If exactly 16 samples are loaded and the address sequences around to channel 0, this address register will never need reloading after each scan.

DAC DATA REGISTER (Write I/O BASE + 4)

15 - 12	11	---	0
Not Used	DAC MSB		DAC LSB

12-bit DAC data are right justified with the most significant bit at bit 11. In bipolar coding, bit 11 indicates polarity (0 = negative, 1 = positive).

SIMULTANEOUS UPDATE REGISTER (Write I/O BASE + 6)

15 - 8	7 - 0
Not Used	x - x

This register has two separate functions. If command bit 6 = 0 and command bit 7 = 1, the analog outputs of all DAC channels will be updated at the same time by writing any value to this register.

If command bit 6 = 1, writing any value to this register will set the trigger ready status flag (status bit 15) to 1. The flag will remain set until cleared to zero by the trigger. This sequence provides a ready/acknowledge handshake to load data frames without losing samples.

CODING TABLE

Input Code (hex)	Output (unipolar)	Output (bipolar)
0FFFh	+Full scale -1 LSB	+Full scale -1 LSB
0801h	1/2 FS +1 LSB	+1 LSB
0800h	1/2 full scale	Zero
07FFh	1/2 FS -1 LSB	-1 LSB
0000h	Zero	-full scale

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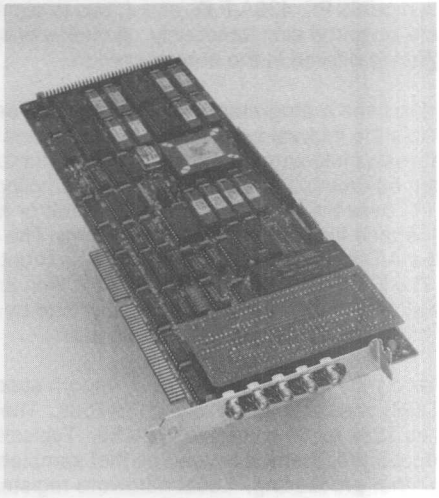
DATEL®
INNOVATION and EXCELLENCE

PC-430
Very High Speed ISA A/D-DSP Coprocessor Board

FEATURES

Now with LabVIEW®

- Up to 10MHz A/D sample rate
- Choice of 12 or 14-bit A/D resolution
- Up to 8Mb dual-ported RAM
- Analog pretrigger ring buffer
- 8k x 32 expansion RAM
- Programmable interrupt to PC/AT host
- 8/16 channel simultaneous sampling optional
- On-board 320C30 40MHz digital signal processor
- On-board DSP library - FFT's, filters, matrix math, floating point, etc.
- Fast, simple, powerful command executive. No local programming required.
- Operates with: IBM-PC/AT®, PS-30, EISA computers and compatibles
- WINDOWS® and Pentium® compatible



GENERAL DESCRIPTION

Advanced performance from the PC-430's on-board Digital Signal Processor (DSP) offers a broad range of high-speed waveform analysis and recording applications. The PC-430 will acquire up to sixteen analog input channels, digitize them and store them in local memory while DSP math processing and data transfer are done concurrently. The system is intended for preprocessing "seamless" A/D data streams to mass storage.

The PC-430 is ideal for non-stop, continuous Fast Fourier Transform (FFT) processing, communications receiver signal collection to disk, or simultaneous graphics display of spectral data. Application areas include signal recovery from noisy channels, harmonic distortion analyzers, and vibration/ resonance filtering systems. For use with ultrasonic, sonar, or acoustic signals, the interrupt-driven, simultaneous block transfers of data ensure no information loss. Other uses include high-speed mapping and imaging, satellite channels, astrophysics, seismology, biomedical signals, array processing, control systems, simulators, engine analyzers, aerodynamics, and vehicle systems.

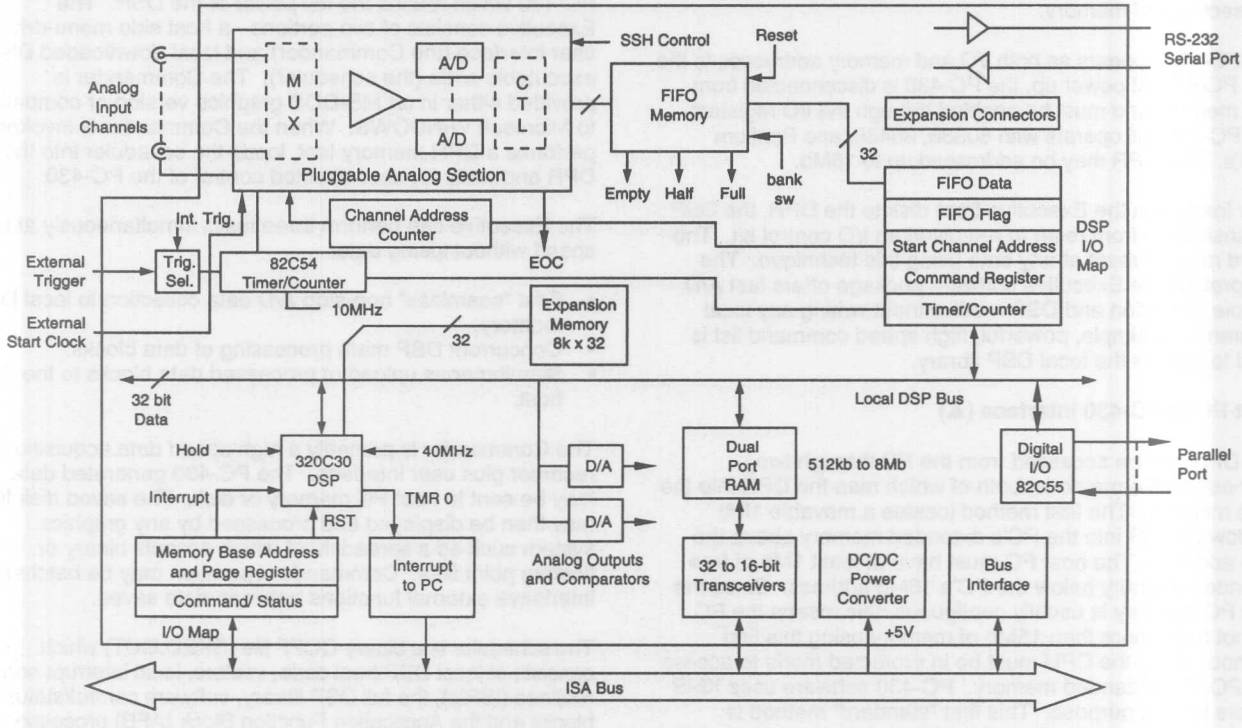


Figure 1. PC-430 Simplified Block Diagram

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Windows is a trademark of Microsoft Corp.
LabVIEW is a trademark of National Instruments

GENERAL DESCRIPTION CONT.

The board consists of a pluggable analog input subsection, timer-counters, DSP central processing unit (CPU), dual port RAM, local RAM, bus interface, registers and DC power supply. On models PC-430A,F,G, and J, two to eight channels are acquired simultaneously. A choice of speeds and resolution is offered in the analog section.

A/D triggering uses a programmable timer-counter section which controls the interval between A/D conversions and the interval between multi-sample A/D scans. The number of samples can be counted for repeating array sampling. The timer-counter uses an on-board crystal oscillator or an external timebase for precision phase-tracking. The digital output of the A/D passes directly to a first-in, first-out (FIFO) memory. The FIFO acts to decouple the precision timing of the A/D section with the block transfers governed by the DSP. Additional internal DSP timers are also used.

A/D FIFO data may be sent to dual port random access memory (DPR) shared with the host PC/ATbus. The DPR is organized as 128k by 32 bits up to 2M x 32. Typically, a swapped dual buffer method is used so that samples are not lost during other processing. Local hardware registers control all A/D, FIFO, and trigger activity.

Single cycle fetch and execution, parallel instructions, zero-overhead of looping instructions, software variable wait states, block repeat and a 64-word internal instruction cache memory are some of the advanced high speed features of the Texas Instruments 320C30 DSP. The DSP uses 32-bit local data paths for very high speed. Data passed to the host PC/ATbus uses 32-to-16 bit transceivers to the DPR. Simultaneous access attempts to the DPR by both the PC/AT host and the DSP are resolved by high speed arbitration logic. The DSP also has a separate 8k by 32-bit local expansion memory for the stack or temporary data. The architecture of the DSP allows simultaneous processing of two tables from two sections of memory.

The PC-430 appears as both I/O and memory addresses to the host PC/AT. At power up, the PC-430 is disconnected from host memory and must be enabled through the I/O registers. The PC-430 will operate with 80386, 80486, and Pentium CPU's. The DPR may be addressed up to 16Mb.

After loading in the Executive from disk to the DPR, the DSP is transitioned from reset to run using an I/O control bit. The board may be reset at any time using this technique. The comprehensive Executive software package offers fast A/D sample collection and DSP math without writing any local programs. A simple, powerful, high speed command list is used to access the local DSP library.

Host PC to PC-430 Interface (▲)

The DPR can be accessed from the PC through two user-selectable methods, both of which map the DPR into the PC's memory. The first method locates a movable 1Mb window of DPR into the PC's extended memory above the 1Mb address. The host PC must have at least 1Mb of free extended memory below the PC's 16Mb address. Since the host PC memory is usually contiguous, this means the PC cannot have more than 15Mb of memory using this first method. Also, the CPU must be in protected mode to access this PC-430 extended memory. PC-430 software uses XMS drivers for this purpose. This first "standard" method is compatible with all previous PC-430 models and with the new enhanced PC-430.

The second method is new to the enhanced PC-430. This method maps a 64kb DPR relocatable window into the PC's memory anywhere below the 16Mb address. Usually in this "paged" mode, the 64kb block will be located below 1Mb where the CPU can access it in real mode. Either access method works with DOS or Windows and both have speed and software tradeoffs. DPR blocks longer than 64kb are accessed by a sliding window technique controlled by an I/O mapped paging register. Both the extended and "paged" memory access methods are supported in DATEL's PC-430 software.

PC-430 SOFTWARE

The following are some methods to control the PC-430:

- Use the PC-430 DATEL Executive software (discussed below).
- Modify the Executive by adding your own code.
- Develop your application from scratch using the TI compiler (and don't use the Executive).
- An integrated DSP display/control/processing system such as PC-430HYPER.
- Use the PC-430LV "bridge" drivers to National Instruments Labview.

Memory Organization

At power up, the entire PC-430 DSP memory is empty (there is no local non-volatile memory). All executable code is downloaded from the host PC disk into the PC-430's Dual Port RAM (DPR). Typically this download is from a TI COFF object file. The host PC does not require any extended memory to be installed for the PC-430 but any existing PC extended memory may be used to collect PC-430 data blocks.

The Executive - Local and Host Sections

DATEL's Executive software offers an easy way to control the PC-430 which retains the full power of the DSP. The Executive consists of two portions - a host side menu-driven user interface (the Commander) and local downloaded DSP executable code (the scheduler). The Commander is provided either in an MS-DOS graphics version or compatible to Microsoft WINDOWS. When the Commander is invoked, it performs a DPR memory test, loads the scheduler into the DPR and waits for user-directed control of the PC-430.

The Executive can perform three tasks simultaneously at high speed without losing data:

- Fast "seamless" non-stop A/D data collection to local DSP memory.
- Concurrent DSP math processing of data blocks.
- Simultaneous upload of processed data blocks to the PC host.

The Commander is primarily a high speed data acquisition recorder plus user interface. The PC-430 generated data may be sent to host PC memory or disk. The saved disk files may then be displayed and processed by any graphics system such as a spreadsheet which accepts binary or floating point files. Commander operation may be batched to interleave external functions between data saves.

The scheduler is a binary COFF file (SKED.OUT) which consists of local DSP boot code, vectors, local interrupt service routines (ISR's), the full DSP library, software control/status blocks and the Application Function Block (AFB) processor.

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FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	PC-430A	PC-430B	PC-430C	PC-430D	PC-430E
Number of Channels	4 Simul.	4	4	1	16SE/8D
Input Configuration (non-isolated)	Single-Ended	Single-Ended	Single-Ended	Differential	SE or Diff.
Full Scale Input Ranges (user-selectable, gain = 1)	0 to +10V ±10V [1]	0 to +10V ±10V ±5V	0 to +10V ±10V ±5V	±5V	0 to +10V ±10V ±5V [1]
Input Bias Current	±1nA	±1nA	±1nA	±1nA	±1nA
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	2µs	2µs	2µs
Common Mode Voltage Range, maximum	—	—	—	±1V	±10V
Input Impedance [Footnote 2]	10MΩ	10MΩ	10MΩ	2kΩ	100MΩ
SAMPLE/HOLD					
Acquisition Time (FSR step, to 0.01% of FSR, max.)	900ns	750ns	200ns	50ns	750ns
Aperture Delay	15ns	20ns	20ns	10ns	20ns
Aperture Delay Uncertainty	±8ps	±100ps	±40ps	±7ps	±40ps
A/D CONVERTER					
Resolution	12 bits	14 bits	12 bits	12 bits	12 bits
Conversion Period	500ns	1.6µs	500ns	200ns	500ns
SYSTEM DC CHARACTERISTICS					
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1	±2	±1
Differential Non-linearity (LSB of FSR)	±0.75	±1	±0.75	±1	±0.75
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.1	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.3	±0.1
SYSTEM DYNAMIC PERFORMANCE					
Input Bandwidth (single channel, FSR input) [Footnote 9]	1MHz	200kHz	1MHz	2.5MHz	200kHz
Throughput to FIFO (single channel, gain = 1)	1.5MHz	500kHz	1.6MHz	5MHz	2MHz
Throughput to FIFO (sequential channels, gain = 1) [Footnotes 4 & 7]	1MHz	330kHz	500kHz	—	500kHz
Total Harmonic Distortion [Footnote 5]	–72dB	–75dB	–72dB	–68dB	–72dB

ANALOG INPUTS	
Programmable Gains	See Footnote 1
Common Mode Rejection (DC - 60Hz)	-80dB (g = 100) (430E)
Addressing Modes	1. Single channel 2. Simultaneous sampling 3. Sequential with autosequenced addressing 4. Random addressing by software

A/D CONVERTER	
Output Coding	Positive-true, right-justified, straight bin. (unipolar) or right-justified 2's comp. (bipolar) with sign extension thru bit 15
Trigger Sources (Software selectable)	1. Local pacer frame clock 2. External TTL frame clock
A/D Sample Clock	1. Internal programmable 82C54 timer 2. Ext. TTL input, active high

FUNCTIONAL SPECIFICATIONS CONTINUED

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	PC-430F	PC-430G	PC-430H	PC-430J [8]
Number of Channels	2 simul.	2 simul.	1	8 simul.
Input Configuration (non-isolated)	Single-Ended	Single-Ended	Differential	Single-Ended
Full Scale Input Ranges (user-selectable, gain = 1)	0 to +10V ±5V	±5V 0 to +10V (separate models)	±5V (other ranges special order)	0 to +2.5V ±5V, ±10V (separate models) [8]
Input Bias Current	±1nA	±1nA	—	±50nA (unipolar version)
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	1µs	—
Common Mode Voltage Range, maximum	—	—	±1V	—
Input Impedance [Footnote 2]	1kΩ	1MΩ	2kΩ	8kΩ (bipolar)
SAMPLE/HOLD				
Acquisition Time (FSR step, to 0.01% of FSR, max.)	165ns	350ns [10]	35ns	400ns
Aperture Delay	20ns	20ns	10ns	—
Aperture Delay Uncertainty	±40ps	±70ps	±3ps RMS	—
A/D CONVERTER				
Resolution	12 bits	14 bits	12 bits	12 bits
Conversion Period	400ns	500ns*	100ns [Footnote 6]	1.6µs (all chans. in simul. sampling)
SYSTEM DC CHARACTERISTICS				
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1.5	±1
Differential Non-linearity (LSB of FSR)	±1	±1	±1	±1
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	±0.15
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	±0.15
SYSTEM DYNAMIC PERFORMANCE				
Input Bandwidth (single channel, FSR input) [Footnote 9]	1MHz	500kHz	5MHz	100kHz
Throughput to FIFO (single channel, gain = 1)	2MHz	1MHz*	10MHz [6]	400kHz
Throughput to FIFO (sequential channels, gain = 1) [Footnotes 4 & 7]	4MHz (2 chans.)	2MHz* (2 chans.)	—	250kHz/chan. (8 chans. simul.)
Total Harmonic Distortion [Footnote 5]	–70dB	–80dB	–65dB	–77dB

*Dual 2MHz 14-bit sampling is available on special order.

FOOTNOTES

1. Resistor-programmed gain from x1 to x100 is available on the PC-430E with increased settling delay at higher gains. Fixed gains of x1 and x10 on 2 channels, offering 1V ranges, are user selectable on the PC-430A.
2. The input impedance of 10 megohms minimum avoids attenuation errors from external input source resistance. For many applications, an in-line coaxial 50Ω shunt, inserted adjacent to the front connectors, is recommended to reduce line reflections and standing wave errors. Input impedance is shown with power on. Impedance with power off is 1500Ω or less.
3. Allow 20 minutes warmup time to rated specifications for models PC-430B,G.
4. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion and FIFO transfer. The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the PC-430C were scanned, the maximum sample rate on any one channel would be 2 microseconds X 4 channels = 8 microseconds (125kHz per channel).

TRIGGER CONTROL	
Programmable Timer Counter Type	82C54 (DSP waits required)
Functions	1. EOC sample counter 2. A/D start rate (16-bit divisor) 3. SSH sample counter (430A only)
Pacer Sample Counter	3 to 65,536 samples.
Clock Source	
Internal	10MHz crystal clock
External	TTL input, direct to A/D
Analog Trigger (▲)	Uses comparator and on-board D/A channel.
Pretrigger (▲)	Sample down - counter is delayed until an external trigger. Pretrigger samples are stored in a ring buffer.

ISA BUS INTERFACE	
Architecture	I/O and memory mapped, for ISA, IBM-PC/AT, PS-30, EISAbus and compatibles.
I/O Mapping	Decodes three 8-bit I/O registers. Decodes I/O address lines A9-A2. 3F0H maximum address.
Data Transfer	Memory block transfer, real or protected mode
Data Bus	16 bits
Number of Interrupts	1 interrupt, software selectable on levels 9, 10, 11, or 15.
Bus Interrupt Sources	DSP interrupt request to PC

LOCAL MICROCOMPUTER	
CPU Type	TI TMS 320C30
Local Data Bus	32 bits
CPU Clock Speed	40MHz
Local DMA Controller	Internal to 320C30 CPU
Primary Memory (Dual access to PC/AT)	128k x 32 static RAM, expandable to 2048k x 32 total (8Mb)
Expansion Memory	8k x 32 static RAM
Internal DSP Memory	Two 1k x 32
Dual Port Access	Hold mode by control bit or from PC/AT dynamic hold per each access.
CPU Test Port	Supports TI XDS1000 Extended Development System.
Local Interrupts to DSP	Int 0-3 from PC host request, A/D FIFO or acquire flags or optional external interrupt.
DSP Wait States	Software programmable up to 7 waits via DSP register
Digital I/O Port (▲)	24 lines, programmable In or Out, TTL levels, 82C55 controller, header connector, typical throughput, 2MHz.

MISCELLANEOUS	
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain
Analog Input Connectors	Four miniature threaded coaxial, type SMA, mounted on rear slot. DB-25 for 430E, J
Trigger Connector (all models except E & J).	5th SMA for external TTL trigger
D/A Analog Outputs (▲)	2 channels, ±5V or ±10V output ranges, 12 bit resolution, 5µs settling. May be used to select analog trigger level.
A/D FIFO Memory (▲)	2048 or 8192 A/D samples, programmable 16 or 32 bits wide.
Memory Expansion Port	Dual-row header connector for 320C30 memory (unbuffered).
Serial Port and External Trigger/Pacer Clock (dual row header)	Two serial channels, compatible to 320C30 serial ports. Both scan (Trigger) and A/D sample clocks are accepted at connector.
RS-232-C Serial Port	3 header pins. Uses software UART.
Operating Temp. Range	0 to +60°C
Storage Temp. Range	-25 to +85°C
Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet. Forced cooling is recommended.
Power Required	+5V dc at 3.5 Amps maximum from ISA bus.
Outline Dimensions	4.2 x 13.2 inches, compatible to ISA bus.

FOOTNOTES CONT.

5. THD test conditions are:
   1. Input frequency: 500kHz (430A,F) 200kHz (430B,E) 300kHz (430C) 1MHz (430D) 100kHz (430G,J) 2MHz (430H)
   2. Generator/filter THD is -90dB minimum.
   3. THD computed by FFT to 5th harmonic.

$$THD = 20 \log_{10} \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}$$

   4. Inputs are –0.5dB full scale. No channel advance.
   5. A/D trigger rate = 1.5MHz (430A), 500kHz (430B,C,E,J), 4MHz (430D), 2MHz (430F), 1MHz (430G), 10MHz (430H)
6. PC-430H: 10MHz sampling may continue until the FIFO memory is full.
7. The PC-430F,G, and J operate in single-channel random address mode or multichannel with automatic channel sequencing. *All* multichannel autosequential models continuously wrap the channel address back to channel zero without delay.
8. PC-430J: models are dedicated as unipolar (0 to +2.5V) or bipolar (±5V, ±10V) input ranges. Pretrimmed gain and offset/zero errors are ±4LSB max. over temp. range. No missing codes guaranteed over temp. range.
9. Full power bandwidth is shown at approximately 3% distortion level. This is not the –3dB amplitude response which is at a higher but non-Nyquist frequency.
10. PC-430G acquisition time is 350ns to ±0.003% of FSR.

PC-430 SOFTWARE CONTINUED

Application Function Blocks

The Executive optimizes three competing objectives:

- Easy to use
- Fast
- Powerful (access to a full DSP software library)

A high speed command list form of control is used to achieve these mutually exclusive goals. The AFB is a short list of commands which call local PC-430 DSP library functions previously downloaded by the Commander to the DPR and resident in the scheduler. No local programming is needed.

Similar to a spreadsheet macro or DOS batch file but much faster, the user writes the AFB file with any text editor and the Commander converts it on the PC side to an internal binary form. The Commander then downloads the converted AFB file to the DPR for execution.

The AFB is powerful because of full access to the DSP library and because repeating functions may be looped. These loops in turn may be nested. Loops can run with a loop count or "forever". Unlike a slow ASCII interpreter, the AFB system runs at nearly the full speed of the 320C30 DSP with minimal overhead. Besides the large DSP library, the user may write additional AFB functions in "C" or TI assembly and integrate them with the scheduler.

AFB Operation

Once the converted AFB file is downloaded to the DPR, the PC-430 generates swapped buffer pairs of data. The PC-430 interrupts the Commander to retrieve these buffer blocks while the alternate buffer is filling with no loss of data. The data blocks may be sent to host memory (fast but limited capacity) and then disk or directly to disk (slower but can use all of available disk).

Buffers can be in any format specified by the AFB - binary integer data, binary float, etc. Either the raw input A/D data may be collected or the results of DSP math operations. All buffer transfers use handshake flags to prevent lost data.

This basic operation may be extended to multiple buffers or interleaved external operation on the PC. To use this environment, the user simply writes the AFB file, sends it to the PC-430 via the Commander then retrieves data blocks. Once the configuration is saved, it can be run from one command line or a batch file.

Commander Operations

The Commander does the following functions:

- Initialize the PC interrupt system to respond to PC-430 buffer ready interrupts.
- Set the PC-430 Extended memory base address and test memory.
- Download the scheduler, DSP library and full local system to the PC-430.
- Boot the PC-430 DSP and confirm operation.
- Allocate PC host memory (either conventional memory or Extended) to receive PC-430 data buffers.
- Edit and compile the user's AFB source file. Your choice of text editor runs underneath the Commander.
- Download a converted AFB file, start execution and retrieve output data files.
- Autorun in batch mode (no menues), display live FFT or time domain graphics, shell out to DOS, and calibrate the A/D.
- Halt the DSP, quit to DOS or WINDOWS.

User-written Extensions

For users writing their own code, the Executive source files provide a rich library of example code. The WINDOWS code includes high performance DLL's (dynamic link libraries) adaptable to other applications.

Multiple external operations may be interleaved between buffer uploads using this simplified sequence:

Start PC-430
LOOP:
  If the previous PC-430 buffer overflowed, report the error.
  Block transfer PC-430 data then swap DPR buffers.
  Do other host tasks (graphics, disk, LAN, D/A, etc.)
  If more data is needed, go to LOOP.

Else, exit

Notice that PC-430 processing continues non-stop during other host processing.

Debugger/Monitor (PC-430BUG)

For users who prefer more direct control of the PC-430 instead of the AFB, optional user programs written in TI "C" or 320C30 assembly language may be run after downloading from the host.

An integrated windowed package consisting of the Debugger (on the PC-430 side) and the Monitor (on the host PC side) offers the following functions:

- Load TI COFF-format object file.
- Display or modify memory (in hex, decimal integer, ASCII, or TI/IEEE floating point).
- Display or modify CPU registers.
- Disassembly memory.
- View file.
- Set, display, or remove breakpoints.
- Go from address until optional breakpoint.
- Single Step DSP, Halt/reset DSP, Block fill.
- Shell out to DOS, Quit to DOS.

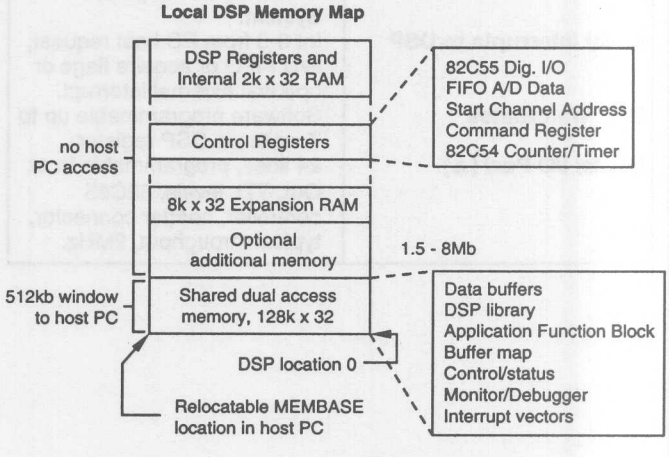


Figure 2. Local DSP Memory Map

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AFB Library Functions

Over 60 functions are included in the Executive AFB library. These are fully described in the PC-430 User's manual (included with the board). The functions become resident when the scheduler is downloaded. Full commented source code to these functions is found in the PC-430SRC and PC-430WINS packages. Most functions are written in mix of high performance "C" and 320C30 Assembly language. Users may modify the functions or add their own functions and rebuild the system.

The functions are grouped in five major categories:

A/D Scan and Timer/Counter Routines

initad, inittim*, sadtsc, sadcr, sstr, sadspc, stads, sfifoi, sadr, rfifo, calad, fifoisr, scommreg.

DSP Array Math Routines

fir, iir, linfir, cirfir, wind*, cfftc, fft, bitrev, twiddle_r, dct, magfft, dbfft, call_sine, call_cos, call_const.

Array Conversion Routines

ieeedsp, dspieee, matadd, matmul, hstgrm, int2flt, sign_extend

Single Variable Transcendentals

sine, cosine, tangent, hyperbolic sine/cosine/tangent, inverse sine/cosine/tangent, square root, powers, exponential, natural logarithm. base_10 logarithm. [These functions are available in the TI "C" library with user-written code.]

Buffer Management

def*, set_ibuf, set_obuf, unrav*, concat, switch_buffers, ibuf_ready, ibuf_release, pause, expenable, expxfer, dprxfer, addxfer, int2pc

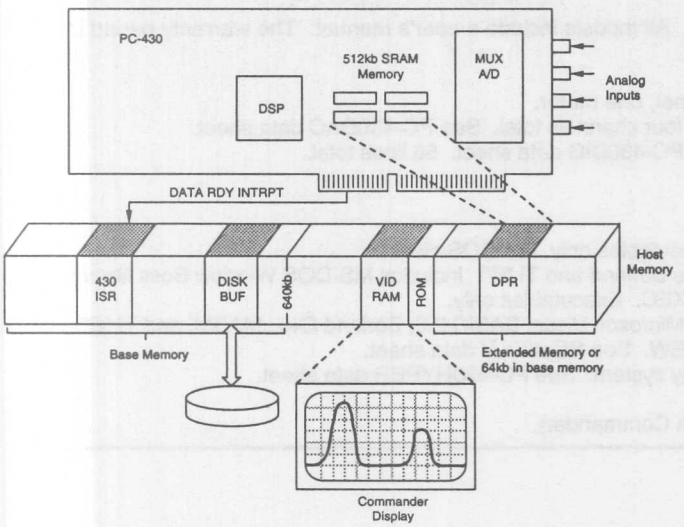


Figure 3. PC-430 Host System Architecture

FIFO DATA FORMAT

A/D data is delivered as a 16 or 32-bit wide stream from the FIFO memory. For multichannel inputs this means that data is multiplexed. For example, on 4-channel inputs, the output channel sequence is 0, 1, 2, 3, 0, 1, . . . Some applications may need this data de-multiplexed by placing each channel's data in separate buffers. Refer to the "UNRAV*" functions.

AFB Source File Format

The AFB source format uses symbolic names for internal PC-430 library functions. The C-like file may be written in free form with the user's choice of loop nesting indentation, skipped lines, etc. Comments after the function name delimiter are ignored. After the user writes the AFB, the PARSE file converter prepares a binary output file which is subsequently downloaded through the Commander for execution.

Here is an AFB example which defines buffers, generates a sine wave, then prepares an FFT array for floating point output:

```
DEFDBUF,            ;function to define double buffer
  0x0L,             ;starting buffer number
  0x400L,           ;buffer length
  0x200L,           ;alignment
DEFSBUF,            ;define single buffer
  0x2L,             ;buffer number
  0x100L,           ;buffer length
  0x100L,           ;alignment
TWIDDLE_R,          ;generate twiddle factors
  0x2L,             ;buffer number 2
BEGIN,              ;begin loop flag
  FOREVER           ;-1 = loop forever flag
CALL_SINE,          ;fill buffer with sine array
  0x00000000L,      ;buffer number 0
  0x00000020L,      ;period of the sine wave
FFT,                ;do FFT on buffer
  0x0L,             ;buffer number 0
  0x200L,           ;number of points
  0x9L,             ;Log 2 of number of points
  0x2L,             ;buffer for twiddle factors
MAGFFT,             ;take magnitude of FFT data
  0x0L,             ;buffer number 0
  0x200L,           ;FFT size
DSPIEEE,            ;convert to IEEE format
  0x0L,             ;buffer number 0
  0x100L,           ;buffer length
SET_OBUF,           ;signal to PC that buffer is ready
  0x0L,             ;buffer 0
  0x100L,           ;buffer length
SWITCH BUFFERS,     ;swap double buffers
END                 ;loop back to BEGIN
END                 ;end of whole AFB
```

PC-430 I/O Registers

I/O Address	Direction	Function
I/O BASE + 0	Write	PC Command Register
	Read	PC Status Register
I/O BASE + 2	Write	Memory Base Address
	Read	Not Used
I/O BASE + 4 (▲)	Write	Page Address Register

Enhanced PC-430

In late 1994, DATEL revised the PC-430 to offer additional features. These are indicated in the specifications by a triangle (▲) and are included by using the extended model number shown in this data sheet. The revised PC-430 is fully downward compatible to existing PC-430's.

The 2Mb memory option now replaces the previous PC-430 plus MEM-30 combination. If you need more than the standard 512kb of DSP memory, use the "2" or "3" designator at the end of this new model number. *Do not use the MEM-30.*

The new memory options are surface mounted. Once selected, they cannot be changed.

Call DATEL for new analog models

Analog Input Ranges (▲)

Certain input ranges are hardware selectable by the user on particular models. The selection is done with jumpers or solder gaps. On other models, the ranges are fixed (they cannot be selected) and these models are noted in the specifications. The polarity designator in the model number is only needed for those models with fixed polarity. For those models that are hardware selectable by the user, the polarity designator in the model number must be set to "A", (default, selection not required), *even if you plan to reconfigure the board to unipolar.* In other words, if the board can be configured for both unipolar and bipolar, use the "A" designator as a model number place holder. For fixed range boards, the "A" means bipolar.

Note: Not all ranges are available on all models. As of this date, the "G" and "J" models *require polarity selection.* Call DATEL if you need ordering assistance.

ORDERING INFORMATION

PC-430 ____ ____ ____ ____

A/D Type, Channels, Resolution	A/D FIFO Size	A/D Polarity	Total On-Board Memory*
A = 4SE simul. chans., 12-bit B = 4SE chans., 14-bit C = 4SE chans., 12-bit D = 1 D chan., 12-bit E = 16SE/8D chans., 12-bit F = 2SE simul. chans., 12-bit G = 2SE simul. chans., 14-bit H = 1D chan., 12-bit J = 8SE simul. chans., 12-bit	1 = 2k samples 2 = 8k samples	A = Bipolar or default, selection not required. B = Unipolar, only for models requiring selection. See "Analog Input Ranges".	1 = 512 kilobytes 2 = 2 megabytes 3 = 8 megabytes *Not including 8k x 32 expansion memory, installed on all models.

Example: PC-430G2A1 - 14 bits, 8k FIFO, bipolar input, 512kb memory.

Each board is power-cycle burned-in, tested, and calibrated. All models include a user's manual. The warranty period is one year.

61-7342340	SMA to BNC cable, one required per channel, one meter.
PC-430DAC	Two additional 12-bit D/A channels. Offers four channels total. See PC-430DAC data sheet.
PC-430DIG	16In/16Out additional digital I/O lines. See PC-430DIG data sheet. 56 lines total.

Software:

PC-430EXEC	Executive, Commander, and Scheduler executables only, MS-DOS disks.
PC-430SRC	Full source code to PC-430EXEC. Requires Borland and TI "C". Includes MS-DOS Window Boss library.
PC-430WIN	Microsoft Windows 3.1 version of PC-430EXEC. Executables only.
PC-430WINS	Full source code to PC-430WIN. Requires Microsoft Visual BASIC 2.0, Borland C++, MASM, and TI "C".
PC-430LV, LVS	Bridge driver to National Instruments LabVIEW. See PC-430LV data sheet.
PC-430HYPER	Hyperception integrated control/store/display system. See PC-430HYPER data sheet.
PC-430BUG	Debugger/monitor and manual.
UM-CMDRSRC	Commander software manual (included with Commander).

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PC-430DAC/PC-430DIG

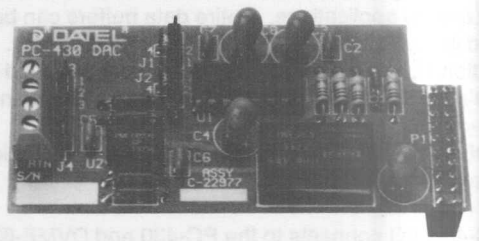
Analog Output and Digital I/O for PC-430 and DVME-630 Boards

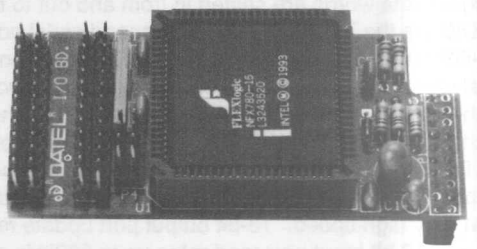
PC-430DAC FEATURES

- **Two analog outputs**
- **12-bit D/A resolution**
- **100kHz D/A update rate**
- **Selectable output voltage ranges**
- **Connects to DATEL's PC-430 and DVME-630 high-performance A/D-DSP boards**

PC-430DIG FEATURES

- **Digital input port - 16 discrete TTL lines**
- **Digital output port - 16 discrete TTL lines**
- **Up to 500kHz data transfer rates**
- **DT-Connect I® compatible connector pinout**
- **Connects to DATEL's PC-430 and DVME-630 high-performance A/D-DSP boards**





GENERAL DESCRIPTION

The PC-430DAC is a high-performance, low-cost, dual-channel analog output module for use with DATEL's PC-430 and DVME-630 high-speed A/D-DSP boards. Applications include system simulation, process control, audio, acoustics, and sonar. The analog outputs can also be used for medium frequency function generation and as programmable voltage sources.

Both channels consist of a 12-bit digital-to-analog converter (DAC) with a maximum settling time of 10µs for full-scale step outputs. Each DAC has an on-chip precision Zener voltage reference and output amplifier. A high-efficiency, low-noise DC/DC converter supplies quiet local analog power. The DC/DC allows four user-selectable full-scale output voltage ranges of ±5V, ±10V, 0 to +5V, and 0 to +10V on both channels. Both outputs are buffered. The D/A data coding can be chosen as straight binary for unipolar voltage applications or two's complement binary for bipolar output ranges.

The PC-430DIG is a high-density 32-line, parallel digital input/output (I/O) daughter module for use with DATEL's PC-430 and DVME-630 high-speed A/D-DSP products. It consists of 16 discrete TTL channels on the input port and 16 discrete TTL output lines on the output port. TTL lines can be written or read independently for complex digital monitoring and control. Applications include process control, digital pattern generation, contact monitoring, logic recording, and parallel digital communications. The digital I/O connector pinout is DT Connect I® compatible to allow easy interfacing to numerous industry-standard hardware port types. An external, active-low TTL input synchronizes data inport reading with external circuits.

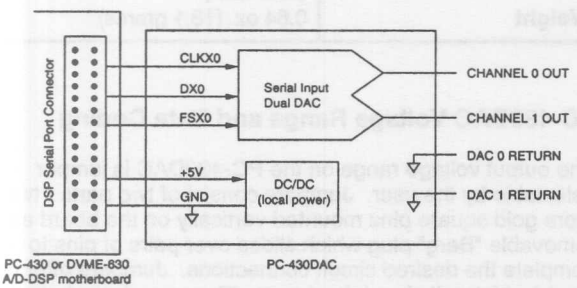


Figure 1 PC-430DAC Block Simplified Diagram

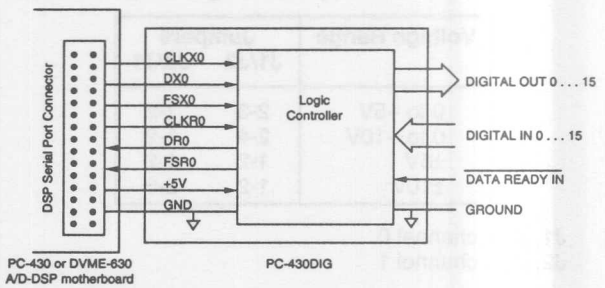


Figure 2. PC-430DIG Simplified Block Diagram

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The PC-430DAC connects to the A/D-DSP motherboard via the high-speed DSP serial port header connector. Serial DAC data is shifted out through the motherboard's TMS320C30 DSP serial port. Bit 13 in each data word selects the output channel. A single data word can be written for DC or slowly varying analog applications. Entire data buffers can be scanned in high-speed control and test environments. Local Application Function Block (AFB) commands supplied in the PC-430 and DVME-630 executive software provide an easy-to-use, no programming control interface to the PC-430DAC. Aggregate channel update rates to 100kHz are possible.

The PC-430DIG connects to the PC-430 and DVME-630 boards via the high-speed DSP serial port header connector. 16-bit digital data words are shifted in from and out to the PC-430DIG via the TMS320C30's high-speed serial port on the A/D-DSP motherboard. Local output port logic converts the serial data stream from the DSP to parallel data words at very high speed. An external Data Ready strobe on the input port latches 16-bit parallel data into a local logic controller and initiates DSP serial port data transfers to the motherboard. Individual samples or complete data buffers can be read or written at very high speed. 16-bit output port update rates to 333kHz and 16 bit input port read rates up to 500kHz are possible. Local AFB functions in the PC-430 and DVME-630 control software allow easy, no-programming access to the PC-430DIG ports.

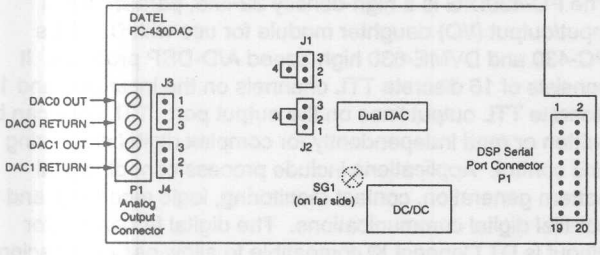


Figure 3. PC-430DAC Board Layout

Table 1. PC-430DAC Output Voltage Range Selection

Voltage Range	Jumpers J1/J2	Jumpers J3/J4
0 to +5V	2-3	1-2
0 to +10V	2-4	1-2
±5V	1-2	1-2
±10V	1-2	2-3

J1, J3 = channel 0
J2, J4 = channel 1

Table 2. PC-430DAC Data Coding Selection

Binary Data Coding	Selection	
Two's complement	Open SG1	(standard)
Straight binary	Close SG1	

PC-430DAC Functional Specifications (Typical at +25°C unless otherwise noted)

ANALOG OUTPUTS	
Number of Channels	2
D/A Resolution	12 binary bits
Output Configuration	Single-ended, non-isolated
Full Scale Output Voltage Ranges	±5V, ±10V, 0 to +10V, 0 to +5V, user-selectable per channel
Output Impedance	0.5Ω
Output Current	5 mAmps max. per channel
Channel Addressing	Individually selectable using bit 13 on each D/A data word
PERFORMANCE	
Monotonicity	No missing codes
Differential Nonlinearity	±0.9 LSB max.
Settling Time	10µs max. (to 0.05% of FSR), 3µs typical
Data Coding	Straight binary or two's complement, user selectable. Data is right justified.
DSP INTERFACE	
Interface	TMS320C30 DSP transmit serial port 0 - FSX0, DX0, CLKX0
Data Transfer Mode	DSP serial port burst mode, non-continuous clocking
Motherboard Connector	20-pin, dual-row internal header - P5 on the DVME-630, P2 on the PC-430
MISCELLANEOUS	
Analog Output Connector	4-pin screw terminal connector. Contains analog output and ground for each channel.
Operating Temp. Range	0 to +60°C
Storage Temp. Range	-25 to +85°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet (0 to 3048 meters)
Outline Dimensions	78mm x 38mm x 20mm (overlaps adjacent PC slot - PC-430 + PC430DAC equals 2 slots total)
Weight	0.64 oz. (18.1 grams)

PC-430DAC Voltage Range and Data Coding

The output voltage range on the PC-430DAC is jumper selectable by the user. Jumpers consist of two parts - two or more gold square pins mounted vertically on the board and a removable "Berg" plug which slides over pairs of pins to complete the desired circuit connections. Jumpers offer high electrical integrity in minimal area. They may be substituted by wire-wrapping the appropriate pins together. The D/A data coding can be selected as straight binary (unipolar output ranges) or two's complement (bipolar output ranges) by closing or opening a solder gap, SG 1. Figure 3 illustrates jumper locations; Tables 1 and 2 list individual selections.

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PC-430DIG Functional Specifications (Typical at +25°C unless otherwise noted)

DIGITAL OUTPUTS	
Number of Output Lines	16
Output Voltage Ratings	V_{OH} 2.4V min., V_{OL} 0.45V max.
Output Current Ratings	I_{OL} 24mA max., I_{OH} -15mA max.
Output Leakage Current	±10µA max.
DIGITAL INPUTS	
Number of Input Lines	16 data plus 1 Ready strobe
Input Voltage Ratings	V_{IH} 2.0V min., 5.3V max. V_{IL} -0.3V min., 0.8V max.
Input Current Ratings	I_{IL} -1.26mA max., I_{IH} 20µA max.
Input Leakage Current	±10µA max.
DSP INTERFACE	
Interface	TMS320C30 DSP transmit and receive serial port 0 - FSX0, DX0, CLKX0, FSR0, DR0, CLKR0
Data Transfer Mode	DSP serial port burst mode, non-continuous clocking
Data Coding	Straight binary, all data is right justified.
Motherboard Connector	20-pin, dual-row internal header - P5 on the DVME-630, P2 on the PC-430
MISCELLANEOUS	
Digital Output Connector(P2)	26-pin dual-row header connector, DT-Connect I® compatible pinout
Digital Input Connector(P3)	26-pin dual-row header connector, DT-Connect I® compatible pinout
Operating Temp. Range	0 to +60°C
Storage Temp. Range	-25 to +85°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet (0 to 3048 meters)
Outline Dimensions	78mm x 38mm x 20mm (overlaps adjacent PC slot - PC-430 + PC430DIG equals 2 slots total)
Weight	1.28 oz. (36.2 grams)

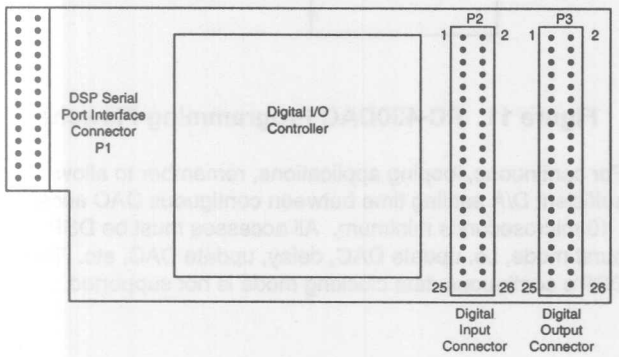


Figure 5. PC-430DIG Board Layout

PC-430DIG/PC-430DAC Installation

The PC-430DIG and PC-430DAC daughter boards both plug onto the high-speed DSP serial port connector on the PC-430 and DVME-630 A/D-DSP products for programming and control. Because both models use the same connector only one of them can be installed in one motherboard at any one time. They are field-pluggable and interchangeable and are installed on the dual-row, 20-pin internal header connector as illustrated in Figures 6 and 7. Both modules require connector clearance and therefore overlay the adjacent PC I/O slot.

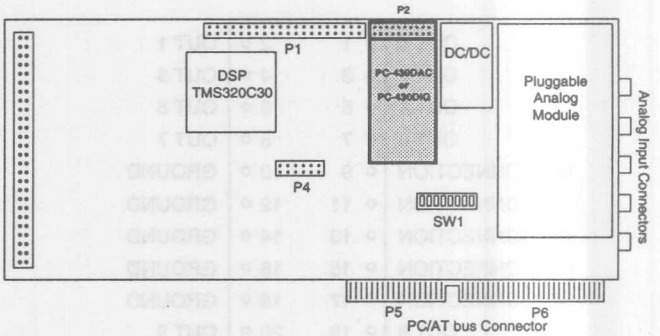


Figure 6. PC-430 Installation

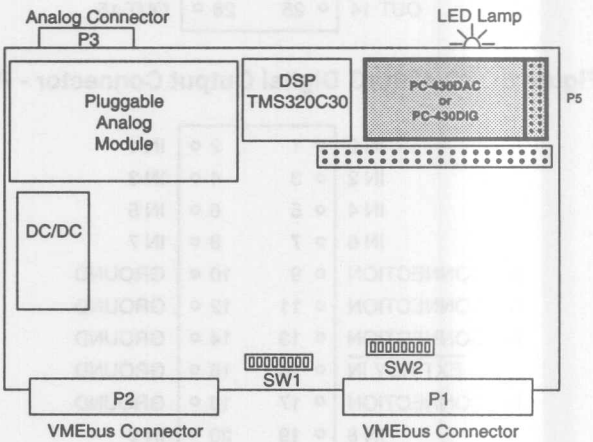


Figure 7. DVME-630 Installation

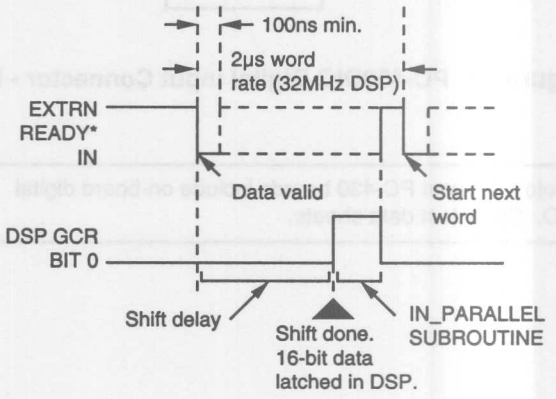


Figure 8. PC-430DIG Ready Strobe Timing

I/O Connector Pinouts

The PC-430DAC analog output connector P1 is a quad screw terminal type used by the two analog output channels and the two corresponding analog returns. Each channel is clearly labeled on the PC-430DAC board layout diagram, Figure 1.

The PC-430DIG includes two 26-pin, dual-row header connectors. P2 is the digital output port and P3 is the digital input port. The connector pinouts are DT Connect I® compatible and are illustrated in Figures 9 and 10.

OUT 0	1	2	OUT 1
OUT 2	3	4	OUT 3
OUT 4	5	6	OUT 5
OUT 6	7	8	OUT 7
NO CONNECTION	9	10	GROUND
NO CONNECTION	11	12	GROUND
NO CONNECTION	13	14	GROUND
NO CONNECTION	15	16	GROUND
NO CONNECTION	17	18	GROUND
OUT 8	19	20	OUT 9
OUT 10	21	22	OUT 11
OUT 12	23	24	OUT 13
OUT 14	25	26	OUT 15

Figure 9. PC-430DIG Digital Output Connector - P2

IN 0	1	2	IN 1
IN 2	3	4	IN 3
IN 4	5	6	IN 5
IN 6	7	8	IN 7
NO CONNECTION	9	10	GROUND
NO CONNECTION	11	12	GROUND
NO CONNECTION	13	14	GROUND
$\overline{\text{EXT RDY IN}}$	15	16	GROUND
NO CONNECTION	17	18	GROUND
IN 8	19	20	IN 9
IN 10	21	22	IN 11
IN 12	23	24	IN 13
IN 14	25	26	IN 15

Figure 10. PC-430DIG Digital Input Connector - P3

Note: Newest PC-430 boards include on-board digital I/O. See latest data sheets.

PC-430DAC Programming

DAC data is shifted out through DSP serial port 0 (FSX0) - MSB first. Due to the PC-430DAC design the serial port registers must be configured for 24 bit word lengths via the DSP's Serial Port Global Control Register. Bit 13 in each DAC data word selects the output channel - 0 or 1. The serial port control, timer, and data registers are memory mapped between DSP addresses 808040 hex and 808048 hex on the PC-430DAC motherboard - DATEL's PC-430 or DVME-630. The TMS320C30 user's manual contains all the necessary register bit field and programming details. The flowchart in Figure 11 illustrates PC-430DAC programming.

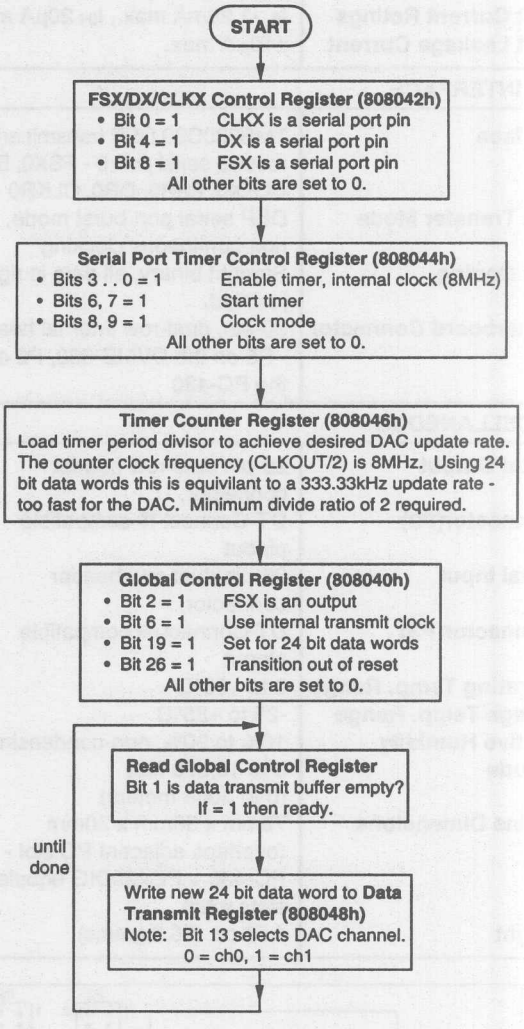


Figure 11. PC-430DAC Programming Flowchart

For continuous, looping applications, remember to allow sufficient D/A settling time between contiguous DAC accesses - 10 microseconds minimum. All accesses must be DSP burst mode, i.e. update DAC, delay, update DAC, etc. The DSP's continuous data clocking mode is not supported.

PC-430DIG Programming

24-bit data is loaded into the Data Transmit Register and is shifted out serially through DSP serial port 0 (FSX0) to the PC-430DIG. The MSB (bit 23) is shifted out first. High-speed local logic on the PC-430DIG buffers the serial data stream and converts it to parallel format. 16-bit parallel input port data is latched into the PC-430DIG on the falling edge of an external data valid input strobe - P3, pin 15. Local logic then converts the data to a serial stream while the DSP reads the data through serial port 0 (FSR0) at the pre-programmed clock rate. The data can be read from the Data Receive Register when bit 0 in the Global Control Register is 1. 16-bit parallel input data rates up to 500kHz are possible using the 32MHz DSP; 16-bit parallel input data rates in excess of 620kHz are possible using the 40MHz DSP.

All DSP serial port control, data, and timer registers are mapped into the TMS320C30's address space between 808040 hex and 80804C hex on the PC-430 and DVME-630 motherboards. The TMS320C30 user's manual contains all the necessary register bit field and programming details. The flowcharts in Figures 12 and 13 illustrate proper PC-430DIG programming.

Application Function Block (AFB) Programming

DATEL's PC-430EXEC and DVME-630EXEC software utilities for the PC-430 and DVME-630 A/D-DSP boards offer a high speed command list form of control that preserves full DSP power. This "no programming" high level text control language is called AFB programming. Full details are available in the PC-430 and DVME-630 data sheets and user's manuals. The AFB executive system offers standard AFB functions to update the PC-430DAC channels and to read/write the PC-430DIG. They include:

OUTDAC	Update a PC-430DAC channel, write a constant or scan from a local buffer.
OUT_PARALLEL	Write the PC-430DIG output port, write one word or scan from a local buffer.
IN_PARALLEL	Read the PC-430DIG input port, read one word or fill a complete buffer.

The AFB system eliminates low level programming without sacrificing hardware performance. The complete source code to the PC-430/DVME-630 commander software and AFB systems is available for users who wish to tailor operation to better suit their application.

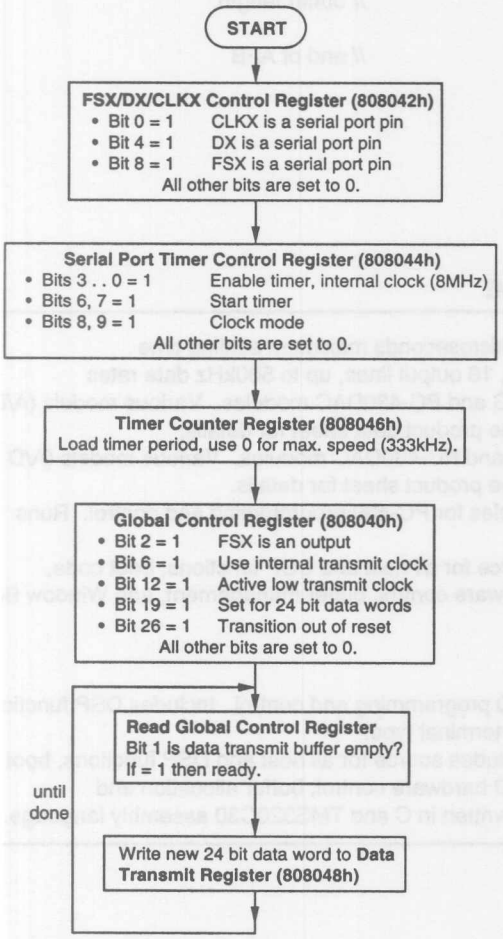


Figure 12. PC-430DIG Output Port Programming

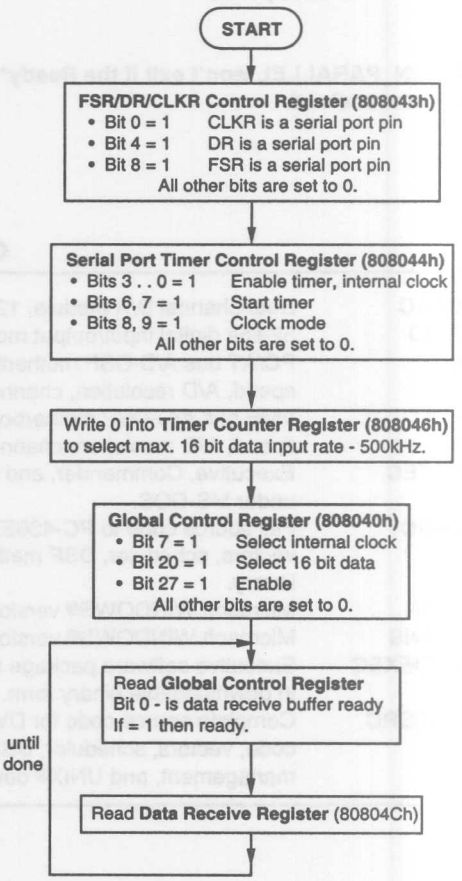


Figure 13. PC-430DIG Input Port Programming

AFB Programming, Continued

All AFB functions are fully documented in the PC-430 and DVME-630 user's manuals. Typical AFB function usage for PC-430DAC and PC-430DIG control is as follows:

```
DEFDBUF,        // define a double buffer
0,              // buffer number 0
1024,           // buffer length = 1k
-1,             // no alignment

DEFDBUF,        // define a double buffer
2,              // buffer number 2
1024,           // buffer size = 1k
-1,             // no alignment

DEFDBUF,        // define a double buffer
4,              // buffer number 4
1024,           // buffer size = 1k
-1,             // no alignment

CALL_CONST,     // load a buffer with a constant
2,              // buffer number 2
15,             // load with constant 15

CALL_COS,       // load buffer with cosine wave
4,              // buffer number 4
8,              // wave period
```

***CAUTION: IN_PARALLEL won't exit if the Ready* Strobe is never received.**

// Read the digital input port on the PC-430DIG

```
IN_PARALLEL*,   // read the input port PC-430DIG
3,              // buffer number where data will be stored
1024,           // read 1024 16 bit words from the port.
                // Reads synchronized by external clock
```

// Write the digital output port on the PC-430DIG

```
OUT_PARALLEL,   // write the PC-430DIG output port
0,              // mode 0 - write data from buffer
5,              // clock rate of 33.33kHz
2,              // data buffer number
1024,           // scan 1024 words
```

// Scan a buffer of data to the PC-430DAC board

```
OUTDAC,         // update a PC-430DAC channel
0,              // DAC channel 0
0,              // mode 0 - write data from buffer
5,              // D/A clock speed of 33.33kHz
4,              // data buffer number 4 - sine wave
1024,           // number of words to scan

SET_OBUF,       // upload buffer to host
3,              // buffer number
1024,           // buffer length

END,            // end of AFB
```

ORDERING GUIDE

PC-430DAC	Dual-channel D/A module, 12-bit resolution, 10 microseconds maximum settling time
PC-430DIG	32-line digital input/output module, 16 input lines, 16 output lines, up to 500kHz data rates
PC-430	PC/AT bus A/D-DSP motherboard for PC-430DIG and PC-430DAC modules. Various models (A/D speed, A/D resolution, channel density, etc.). See product data sheet for details.
DVME-630	VME bus A/D-DSP motherboard for PC-430DIG and PC-430DAC modules. Various models (A/D speed, A/D resolution, channel density, etc.). See product sheet for details.
PC-430EXEC	Executive, Commander, and Scheduler executables for PC-430 programming and control. Runs under MS-DOS.
PC-430SRC	Full source code to PC-430EXEC. Includes source for all host and DSP functions, boot code, vectors, scheduler, DSP math libraries, A/D hardware control, buffer management, and Window Boss library.
PC-430WIN	Microsoft WINDOWS® version of PC-430EXEC.
PC-430WINS	Microsoft WINDOWS® version of PC-430SRC.
DVME-630EXEC	Executive software package in "C" for DVME-630 programming and control. Includes DSP functions in downloadable binary form. Uses VT-100 host terminal type.
DVME-630SRC	Complete source code for DVME-630EXEC. Includes source for all host and DSP functions, boot code, vectors, scheduler, DSP math libraries, A/D hardware control, buffer allocation and management, and UNIX® device drivers. Code written in C and TMS320C30 assembly language.

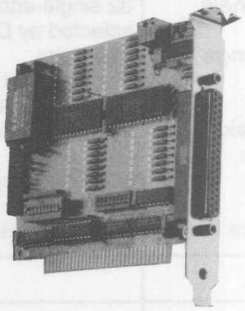
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PC-440
32-Channel, Analog Input Expansion Board for IBM-PC

FEATURES

- **32 single-ended/16 differential expansion channels**
- **Use with DATEL's PC-411/PC-412 boards**
- **Cascadable to 512 channels (SE) or 256 channels (D)**
- **Channel select by PC bus or digital input port**
- **10 microseconds settling time**
- **Local programmable gain amplifier (PGA)**
- **Optional signal conditioning pads**
- **On-board DC/DC power converter**



GENERAL DESCRIPTION

The PC-440 is a channel expansion board for use with any A/D board on IBM-PC, PC/XT, PC/AT, EISA bus, and compatible computers. It interfaces to DATEL's PC-411/412 family of multifunction I/O boards. Each PC-440 offers 32 single-ended or 16 differential analog input channel expansion capability and multiple boards can be cascaded to achieve a very high channel expansion for one A/D board. Each channel in the system is multiplexed down to the A/D converter on the parent A/D board where it is digitized for further processing, storage, or display on the host computer.

Base address switches select each board's I/O address. Up to eight PC-440's can be mapped to one I/O base address location when operating in single-ended mode, up to 16 in differential mode. Since there are 256 individual I/O address locations decoded by the PC-440, the total number of externally multiplexed channels per A/D board is extremely large. Channel addresses can be generated by software on the host computer or can be loaded from the digital input port. For channel scan applications, the channel address can be advanced by a software strobe or an external TTL input.

The input voltage range is ±10 Volts. Optional circuit pads on each channel may be configured for other voltage ranges, for current loop inputs, or for analog signal conditioning. The on-board Programmable Gain instrumentation Amplifier (PGA) is user-selectable for gains from 1 to 100 to accommodate low level inputs. It may be bypassed to minimize channel settling delays. A local dc-to-dc converter supplies all the analog power required from the PC/XT/AT bus +5 Volt line.

The PC-440 is configured on a half-size PC/XT/AT ISAbus card and plugs directly into the host computer bus via the I/O expansion connectors. Analog signal field connections are made through a 37-pin 'D-type' connector on the rear mounting bracket. Connections are made to the digital input port via a 26-pin, male header connector mounted internally on the PC-440. This connector also contains the analog output signals from the multiplexer and the PGA.

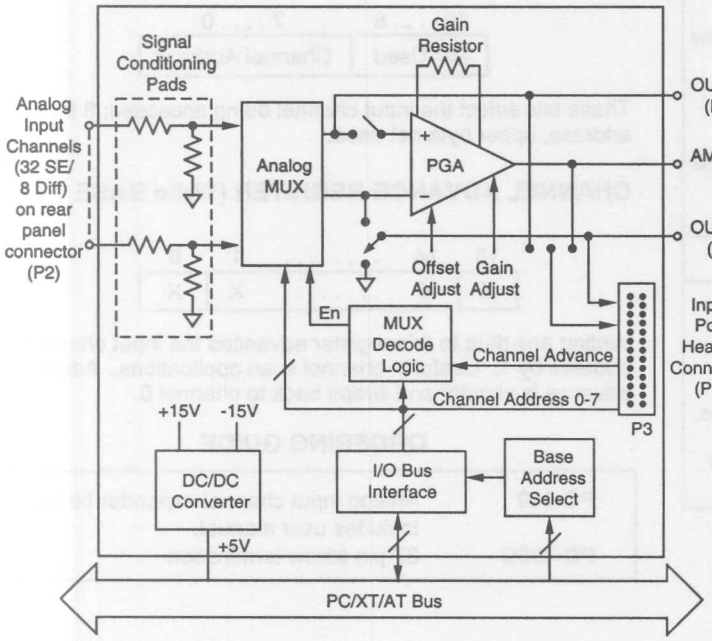


Figure 1. PC-440 Simplified Block Diagram

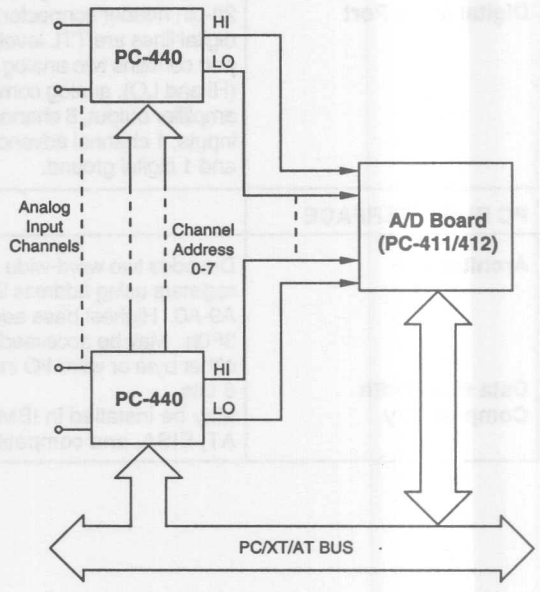


Figure 2. Interfacing PC-440 to A/D Board

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SPECIFICATIONS (Typical at +25°C unless noted)

ANALOG INPUTS	
Number of Channels	32 single-ended or 16 differential, selected by DIP switch
Input Voltage Range	±10 Volts
Configuration	Non-isolated break before make
Overvoltage	±20V max. sustained no damage
Channel OFF Leakage	±30 picoAmps
Channel ON Bias Current	±50 nanoAmps
Channel OFF Input Capacitance	5 picoFarads
PERFORMANCE	
Linearity	±0.01%
Crosstalk (1 kHz FS)	±0.005%
Settling Time (no PGA)	2 microseconds maximum
Settling Time to 0.01% PGA Gain = 1	10 microseconds maximum
Settling Time to 0.1% PGA Gain = 100	40 microseconds maximum
Programmable Gain	1 to 100, selected with user-installed precision resistor. Same gain fixed for all channels.
Temp. Coefficient of Gain	±20ppm of FSR per °C
Temp. Coefficient of Zero	±15ppm of FSR per °C
DIGITAL CONTROL	
Channel Address	8-bit address code may be loaded from bus or digital input port.
Address Page Offset	Channel banks may be selected per board - up to 8 SE, up to 16 DIFF. Multiple PC-440's can share the same I/O base address. Deselected PC-440's disconnect their channel MUX to share an output line.
Channel Advance	1. Software strobe or 2. External TTL input, active low
Digital Input Port	26-pin header connector. All digital lines are TTL levels. The port contains two analog outputs (HI and LO), analog common, amplifier output, 8 channel address inputs, 1 channel advance input, and 1 digital ground.
PC BUS INTERFACE	
Architecture	Decodes two word-wide I/O registers using address lines A9-A0. Highest base address is 3F0h. May be accessed with either byte or word I/O instructions.
Data Bus Width	8 bits
Compatibility	May be installed in IBM-PC, XT, AT, EISA, and compatibles

MISCELLANEOUS	
Connectors	PC bus, 62-pin edgeboard. Input port, 26-pin header suitable for flat cable. Analog input, DB-37 rear panel connector
Switches	Two Dual Inline Package (DIP): I/O base address, page map offset, PGA in/out, single-ended/differential modes
Adjustments	PGA Offset and Gain
Operating Temp Range	0 to +60°C
Storage Temp Range	-25 to +85°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet
Power Required	+5Vdc and 1 Amp maximum from PC bus
Outline Dimensions	4.2 x 5.3 x 0.5 inches (10.5 x 13.3 x 1.3 cm)
Weight	5 ounces (195 grams)

PROGRAMMING

The PC-440 I/O base address may be selected up to 3F0 hex on 4 byte boundaries. The board decodes two 16-bit I/O registers as follows:

I/O Address (Hex)	Direction	Description
BASE + 0	Write	Channel Address Register
BASE + 2	Write	Channel Advance Register

If multiple boards share the same base address, channel banks are selected with on-board DIP switches; details in user manual.

CHANNEL ADDRESS REGISTER (Write BASE + 0)

15 8	7 0
Not Used	Channel Address

These bits select the input channel being accessed; 8 bit address, upper byte not used.

CHANNEL ADVANCE REGISTER (Write BASE + 2)

15	14	. . . . .	1	0
X	X	. . . . .	X	X

Writing any data to this register advances the input channel address by 1. Useful in channel scan applications. Address advance is circular and wraps back to channel 0.

ORDERING GUIDE

PC-440	Analog input channel expander board. Includes user manual.
PC-490C	37-pin screw termination

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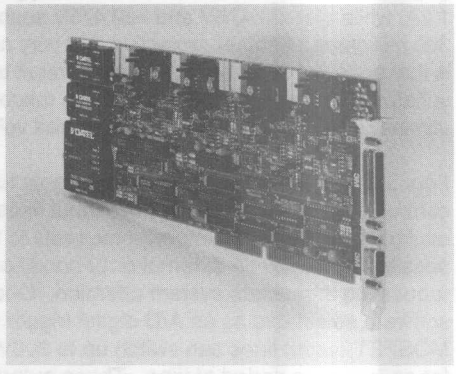
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INNOVATION and EXCELLENCE

PC-462
Precision Programmable Power Supply Board

FEATURES

Now with LabVIEW®!

- 4 independently programmable, precision voltage/current outputs
- Remote sensing for all supplies
- All channels fully isolated from PC/ATbus
- Output current limits
- Real time voltage and current monitoring
- 4 general purpose analog inputs
- 2 isolated digital inputs
- 2 isolated relay driver outputs - MOSFET switches
- Comprehensive software, free driver library



GENERAL DESCRIPTION

Designed for low-cost, medium power source applications, the PC-462 is a high-precision, programmable power supply and sensing board for IBM-PC/AT, PS-30, EISAbus and compatible computers. Four output channels are individually programmable for ranges of 0 to +6.1425V and 0 to –6.1425V at 1A, as well as 0 to +20.475V and 0 to –20.475V at 250 millamps. It is ideal for applications where highly accurate, very stable DC voltage and current sources are required, with low ripple and low noise characteristics. All input and output channels provide 250Vrms isolation from the PC/ATbus. Combined with comprehensive, graphic-intensive control software, this quad output supply card is easily integrated into most automated test and benchtop power supply applications.

For dynamic test sequences, the host PC can update all four output channels in real time. Voltage and current output levels are continuously monitored by an on-board, 12-bit A/D converter. A rear panel connector provides an additional 4 auxilliary input channels for general purpose use. The input range is ±5.12V but component pads on all of the channels allow for user-selectable ranges as well as current loop inputs and signal filtering. These channels are fully isolated from the PC/ATbus and are ideal for monitoring external voltage/current conditions in adaptive test applications.

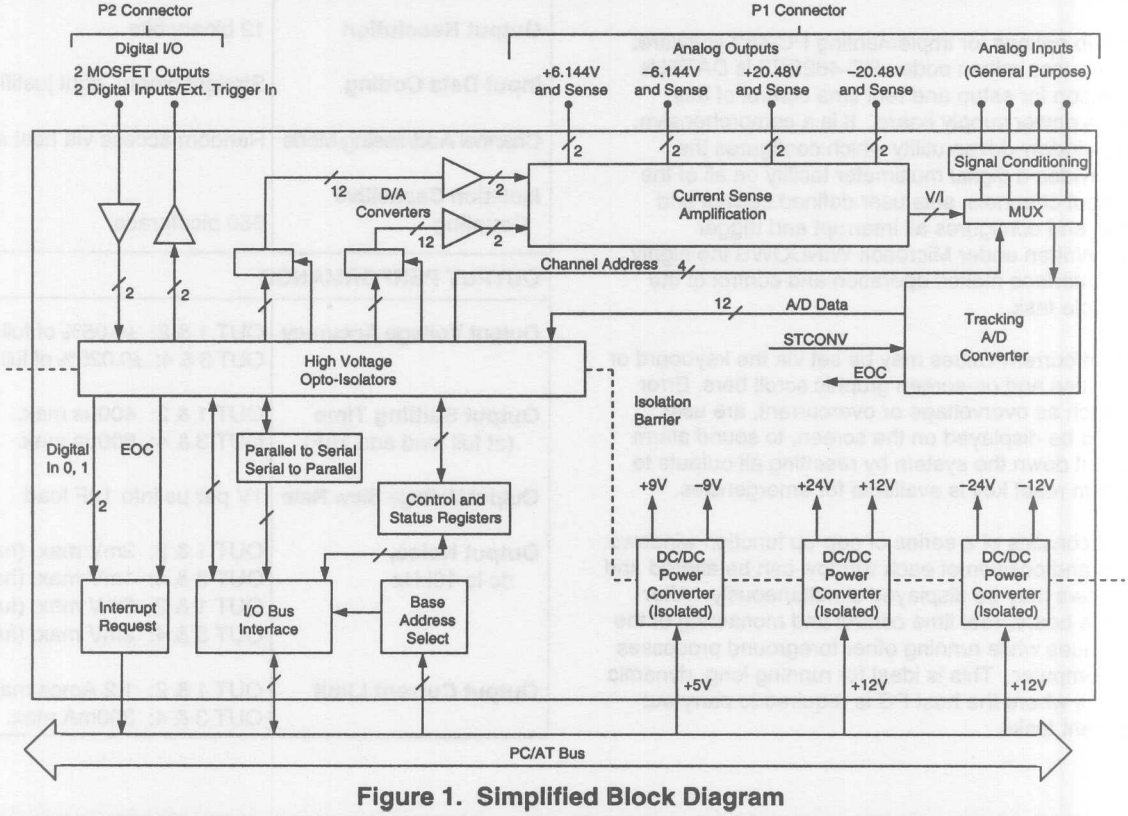


Figure 1. Simplified Block Diagram

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GENERAL DESCRIPTION (Continued)

Outputs are protected against overload and short circuit damage by fixed current limiting circuits. For any overload condition, the +6.1425V and –6.1425V supplies are limited to 1.2A, while the +20.475V and –20.475V supplies are limited to 300 milliamps. Another protective and very necessary feature is that at power up all output channels reset to 0V. Remote voltage sensing permits regulation with respect to the load eliminating problems associated with lead voltage drops.

Four isolated digital I/O lines are available to monitor and control external devices. The two input lines may be configured to generate interrupt requests to the host computer possibly indicating an external error condition or failure and requesting immediate system attention. One of these lines is software selectable as an A/D digital trigger input. The two MOSFET output lines can switch up to 300V at 100 milliamps for an indefinite period of time. These outputs are ideal for switching heavy external loads such as relays, triacs, etc.

The PC-462 is configured on a full size, PC/AT card and it is completely contained within the host computer. The direct bus interface increases the output slew rates and decreases the host response time to read back voltage/current data. All isolated input and output channels are available on two D-type connectors on the rear panel. The board is compatible with most popular programming languages and all data is right justified to facilitate integer data typing with high level languages such as C, FORTRAN, Pascal, or Ada. A comprehensive User's Manual details full installation, programming, and application information.

SOFTWARE

Users have two options for implementing PC-462 software: PC-462SET or user written code. PC-462SET is DATEL's complete solution for setup and real time control of this programmable power supply board. It is a comprehensive, easy-to-use, window-driven utility which configures the hardware, provides a digital multimeter facility on all of the input and output channels, sets user defined current and voltage limits, and configures all interrupt and trigger procedures. Written under Microsoft WINDOWS the highly graphic user interface makes operation and control of the PC-462 a simple task.

Output voltage/current values may be set via the keyboard or by using a mouse and on-screen graphic scroll bars. Error conditions, such as overvoltage or overcurrent, are user configurable to be displayed on the screen, to sound alarm bells, or to shut down the system by resetting all outputs to zero. A system reset key is available for emergencies.

The package consists of a series of pop-up function windows. Both the size and position of each window can be altered and multiple windows may be displayed simultaneously. After configuring the board, real time control and monitoring of the PC-462 continues while running other foreground processes on the host computer. This is ideal for running long, dynamic test sequences where the host PC is required to carry out other concurrent tasks.

For custom applications, the User's Manual contains detailed register and timing information as well as example software routines necessary to help users to develop their own code - in any programming language. The PC-462 is supplied with a low-level device driver library written in C and supplied on MS-DOS diskettes. The library may be incorporated into user programs and used for configuring and controlling the PC-462. Also, the complete source code listing (PC-462SRC) for PC-462SET is available from DATEL on 3.5" MS-DOS diskettes to further facilitate software development.

SPECIFICATIONS

(Typical at 25°C, dynamic conditions, unless noted)

ANALOG OUTPUTS	
Number of Channels	4
Output Configuration	Single-ended, common isolated analog ground
Full Scale Output Ranges (See Notes 1 & 4)	OUT 1 0 to +6.1425V @ 1 Amp OUT 2 0 to –6.1425V @ 1 Amp OUT 3 0 to +20.475V @ 250mA OUT 4 0 to –20.475V @ 250mA
Isolation	250Vrms isolation to PC/ATbus
Isolation Resistance	10 Megohms
Output Resolution	12 binary bits
Input Data Coding	Straight binary, right justified
Channel Addressing Mode	Random access via host software
Isolation Capacitive Coupling	850 picofarads
OUTPUT PERFORMANCE	
Output Voltage Accuracy	OUT 1 & 2: ±0.05% of full scale OUT 3 & 4: ±0.025% of full scale
Output Settling Time (at full load and 1µF)	OUT 1 & 2: 400µs max. OUT 3 & 4: 600µs max.
Output Voltage Slew Rate	1V per µs into 1µF load
Output Noise, dc to 10kHz	OUT 1 & 2: 2mV max. (half load) OUT 3 & 4: 1mV max. (half load) OUT 1 & 2: 5mV max. (full load) OUT 3 & 4: 2mV max. (full load)
Output Current Limit	OUT 1 & 2: 1.2 Amps max. OUT 3 & 4: 300mA max.

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OUTPUT PERFORMANCE (Continued)	
Output Stability	Unconditionally stable into any load
Transient Response (Half Load Change)	200 microseconds maximum
Temp. Coefficient of Gain	±20ppm of FSR per °C
Temp. Coefficient of Offset	±20ppm of FSR per °C

ANALOG INPUTS	
Number of Channels	12 dedicated to internal measurements, 4 general purpose
Dedicated Channels	CH 0 OUT 1 Voltage monitor CH 1 OUT 1 Current monitor CH 2 OUT 2 Voltage monitor CH 3 OUT 2 Current monitor CH 4 OUT 3 Voltage monitor CH 5 OUT 3 Current monitor CH 6 OUT 4 Voltage monitor CH 7 OUT 4 Current monitor CH 8 +5.12V Ref. monitor CH 9 –5.12V Ref. monitor CH 10 GND CH 11 GND
General Purpose External Channels	Channels 12, 13, 14, and 15
Analog Input Range	±5.12V (see Tech. Note 2)
Input Configuration	Isolated, 250Vrms channel to PC/ATbus
DC Accuracy	±0.025% of full scale (plus ±1LSB at 12 bits)
Input Impedance (See Tech. Note 3)	10 megohms minimum
Input Bias Current	±500 nanoamps
Input Capacitance	1000pF in series with 2 kilohm resistor
Input Overvoltage	±6V sustained max., no damage
Addressing Modes	Random via host software

A/D CONVERTER	
Resolution	12 binary bits
Conversion Time	50 microseconds
Output Coding	Straight binary; 11 data bits, 1 sign bit (MSB)
A/D Trigger Source	Initiated via host software or by external TTL input
External Trigger Pulse Width	20µs min., active low. TTL levels on digital input line 0.

DIGITAL INPUTS	
Number of Channels	2
Isolation	250Vrms to PC/ATbus
Input Current	0mA OFF, 10mA ON, TTL levels
Input Bandwidth	50kHz

DIGITAL OUTPUTS	
Output Type	MOSFET power switches, passive.
Number of Channels	2 channels, high voltage and current capability for switching heavy loads
Output Ratings	300V, 100mA continuous. External excitation required.
Isolation	250Vrms to PC/ATbus, MOSFET switches
Switch ON Resistance	25 Ohms
Switch Time	ON 1 millisecond OFF 1 millisecond

PC-ATBUS INTERFACE	
Architecture	I/O mapped, pluggable to IBM-PC/AT, PS-30, EISAbus and compatible computers. Decodes four 16-bit I/O registers.
I/O Mapping	Decodes I/O address lines A9 through A3. A2..A0 are decoded on-board for individual register access. Highest base address is 3F8 hex.
Data Bus	16-bit I/O transfers, all data is right justified

PC/ATBUS INTERFACE (Continued)	
PC/ATbus Interrupt	1 line, software selectable on IRQ 10, 11, 12, or 15
Bus Interrupt Sources	Software selectable as: 1. A/D End Of Conversion (EOC) 2. Digital input channel 0 low 3. Digital input channel 1 low
CONNECTORS	
Analog Connector, P1	25-pin female, DB-25S connector on rear mounting bracket for easy access to precision voltage and sense outputs and general purpose analog inputs.
Digital I/O Connector, P2	9-pin female, DB-9S connector on rear mounting bracket. Includes +5V system power connection.
MISCELLANEOUS	
Power Requirements (See Tech. Note 4)	4 Amps max. from PC/ATbus +5V 1.5 Amps max. from PC/ATbus +12V
Operating Temp	0 to +50°C
Storage Temp Range	–25 to +80°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 ft (0 to 3047 meters). Forced cooling is recommended.
Outline Dimensions	4.5" H x 13.31" L x 0.5" W (11.43 x 33.81 x 1.59 cm), full size PC/AT board. Uses a single PC/AT slot.
Weight	0.466kg (1 pound)

TECHNICAL NOTES

1. All outputs reset to 0V at power up. The output voltage steps on each supply are:

OUT 1 and OUT 2	1.5 millivolts per LSB
OUT 3 and OUT 4	5.0 millivolts per LSB

2. Users can select different voltage ranges for this general purpose analog input channel by inserting attenuation resistors into component pads provided. Capacitors mounted in these pads can provide signal filtering. Discrete components needed for current loop inputs would mount in these pads as well.

3. The input impedance of 10 megohms minimum avoids attenuation errors due to external source resistances.

4. Power requirements are specified with all outputs driving FULL loads. At full load on all channels, the maximum total power required is 40 Watts. At half load it is 20 Watts, at quarter load 10 Watts, etc. 1.5 Amp maximum current can be drawn from OUT 1 and OUT 2.

5. Recalibration is recommended at 90 day intervals, depending on operating conditions.

PROGRAMMING NOTES

(Refer to PC-462 User's Manual for detailed programming information)

1. Since all registers are I/O mapped, I/O read and write commands must be used. For example, in C, 'outport' will write a 16-bit word to the specified register address while 'inport' will read a 16-bit word from that register.

2. When setting a value on an output channel, command and address information must be written before writing DAC data.

3. The PC-462 may be programmed in almost any high- or low-level language. The following example program illustrates how to set an output channel's value:

```
#define BASE 0X300  /* User-defined base address*/

#include <stdio.h>
#include <math.h>

main ( )
{
        unsigned short channel_addrs_reg, dac_data_reg;
        int channel, dac_data;
        float volts, full_scale;

        channel_addrs_reg = BASE + 2;
        dac_data_reg = BASE + 4;

        printf ("Which channel (0. . .3) =>  ");
        scanf ("%d, &channel);

        printf ("Output voltage =>  ");
        scanf ("%f", &volts);

        outport (channel_addrs_reg, channel );

        switch (channel)    /* Set channel full scale */
        {                   /* output voltage levels */

        case 0:
        case 1:     full_scale = 6.1425;
                    break;
        case 2:
        case 3:     full_scale = 20.475;
                    break;
        }

        dac_data = (int) (fabs (volts) * 4096.0/full_scale);

        outport (dac_data_reg, dac_data);  /*Update channel */

        return (0);
}
```


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PROGRAMMING NOTES (Continued)

4. Note that DAC data may be entered from a keyboard, it may be generated in software, or it may be played back from a user-created disk file.

5. Load overvoltage/overcurrent conditions may be monitored in real time by selecting the A/D converter input channel and then polling the A/D data register. The ideal situation is to continuously scan each of the output channels using software.

6. Monitor external system error conditions by configuring one of the two digital input lines as an interrupt request to the host PC. On error, shut the system down by resetting all the outputs to 0V. Status polling may not detect the exact instant that an error occurs.

7. A/D scanning of the dedicated channels or general purpose auxilliary channels may be stepped along in software or by an external digital trigger input. Synchronize software initiation by having the time of day clock interrupt the CPU periodically.

I/O REGISTER MAP

The base address may be selected anywhere up to 3F8 hex, on 8-byte boundaries. At power-up, all control registers contain zeroes and all output channels reset to 0V. The DAC data register may be written after programming the channel address and command modes. 16-bit I/O word instructions must be used. Unlisted registers are not used. DAC register (BASE + 4) data must be integer format and must be scaled relative to a channel's full scale output voltage range - see Programming Note 4.

I/O Address (hex)	Direction	Description
BASE + 0	Write	Command Register
BASE + 0	Read	Status Register
BASE + 2	Write	Channel Address Register
BASE + 4	Write	DAC Data Register
BASE + 6	Write	Conversion Register Start A/D
BASE + 6	Read	A/D Data Register

COMMAND REGISTER (Write I/O BASE + 0)

15 – 8	7 6 5	4 3	2	1 0
Not Used	Intrpt Level 2 1 0	Intrpt Source 1 0	Trig Select	Digital Outport 1 0

Digital Outport (Bits 1, 0) — Isolated digital MOSFET output bits. Can be used for normal switch applications or for driving power relays when switching heavier loads.

Trigger Select (Bit 2) — This bit selects the A/D converter trigger source as follows:

- 0 Internal trigger - write to A/D start conversion register (Write BASE + 6)
- 1 External trigger - active low signal on digital input line DIG IN 0 initiates one A/D conversion on the selected channel. A/D channel selection is made by writing bits 7 through 4 in the channel address register. 20 microseconds minimum trigger pulse width.

Interrupt Source Select — Bit 4 3

- 1 1 Interrupt on End of A/D Conversion (EOC)
- 0 1 Interrupt when Digital Input 0 low
- 1 0 Interrupt when Digital Input 1 low
- 0 0 Not used

Interrupt Level Select — Bit 7 6 5

- 0 0 0 Disable Interrupts
- 0 0 1 Interrupt on IRQ 10
- 0 1 0 Interrupt on IRQ 11
- 0 1 1 Interrupt on IRQ 12
- 1 0 0 Interrupt on IRQ 15
- 1 0 1 Not Used
- 1 1 0 Not Used
- 1 1 1 Not Used

STATUS REGISTER (Read I/O BASE + 0)

15 – 8	7 6 5	4 3	2	1 0
Not Used	Interrupt Level Status 2 1 0	Interrupt Source Status 1 0	EOC Status	Digital Inport 1 0

Digital Inport (Bits 1, 0) — Isolated digital input bits. These may be used as general purpose TTL input lines or to generate interrupt requests to the host PC from an external event, e.g. overcurrent or overvoltage.

EOC Status (Bit 2) — 0 = A/D conversion in progress, data invalid
1 = A/D conversion done, data valid

EOC is a 7 microsecond wide, active high pulse and occurs at the end of each A/D conversion.

Status Bits (Bits 7 . . 3) — Follow the corresponding bits in the command register.

Status Bits (Bits 15 . . 8) — Not used

CHANNEL ADDRESS REGISTER (Write I/O BASE + 2)

15 – 8	7 6 5 4	3 2	1 0
Not Used	A/D Channel Select 3 2 1 0	Not Used	D/A Channel Select

D/A Channel Select (Bits 1,0)

Bit 1	0	
0	0	Select OUT 1 for update (0 to +6.1425V)
0	1	Select OUT 2 for update (0 to –6.1425V)
1	0	Select OUT 3 for update (0 to +20.475V)
1	1	Select OUT 4 for update (0 to –20.475V)

Bits 3, 2 — Not used

A/D Channel Select (Bits 7 - 4)

Bit 7	6	5	4	
0	0	0	0	OUT 1 Voltage monitor
0	0	0	1	OUT 1 Current monitor
0	0	1	0	OUT 2 Voltage monitor
0	0	1	1	OUT 2 Current monitor
0	1	0	0	OUT 3 Voltage monitor
0	1	0	1	OUT 3 Current monitor
0	1	1	0	OUT 4 Voltage monitor
0	1	1	1	OUT 4 Current monitor
1	0	0	0	+5.12V Reference monitor
1	0	0	1	–5.12V Reference monitor
1	0	1	0	Ground
1	0	1	1	Ground
1	1	0	0	Isolated analog input channel 0
1	1	0	1	Isolated analog input channel 1
1	1	1	0	Isolated analog input channel 2
1	1	1	1	Isolated analog input channel 3

Bits (15 - 8) — Not used

DAC DATA REGISTER (Write I/O BASE + 4)

15 – 12	11	10 — 1	0
Not Used	DAC 1 (MSB)	DAC Data Bits 2 through 11	DAC 12 (LSB)

12-bit DAC data is right justified with the Most Significant Bit (MSB) at bit 11. The MSB is referred to as DAC bit 1. The Least Significant Bit (LSB) is DAC 12. Writing to this register always updates the selected channel.

START CONVERSION REGISTER (Write I/O BASE + 6)

15	14	1	0
X	X	X	X

'X' indicates don't care bit

Writing any data value to this register starts an A/D conversion on the channel specified by bits 7 through 4 in the channel address register.

A/D DATA REGISTER (Read I/O BASE + 6)

15 – 12	11	10 — 1	0
0 – 0	AD 1 (MSB)	A/D Data Bits 2 through 11	AD 12 (LSB)

The host reads 12-bit A/D data from this register. All data is right justified. The upper 4 bits are zeroed. A/D data is read from one of the internal voltage/current monitor signals or from one of the 4 general purpose external analog channels. The analog source is specified in the channel address register.

REAR PANEL INPUT/OUTPUT CONNECTIONS

All input and output connections are made using two female connectors on the rear mounting panel. P1 is a 25-pin, DB-25S connector for all load connections to the PC-426 output channels. P1 also includes the four auxilliary, general purpose analog input connections.

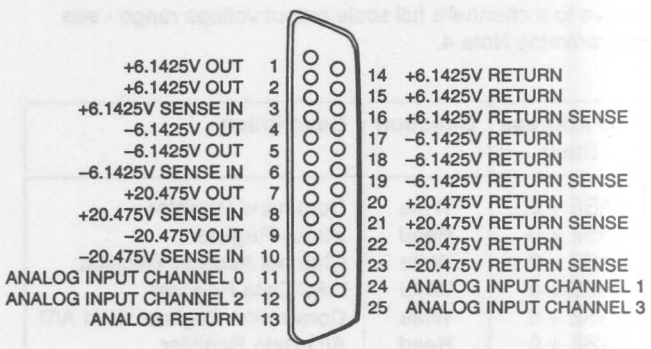


Figure 2. Voltage/Current Outputs, Analog Inputs - P1

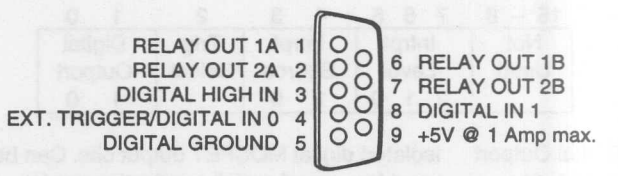


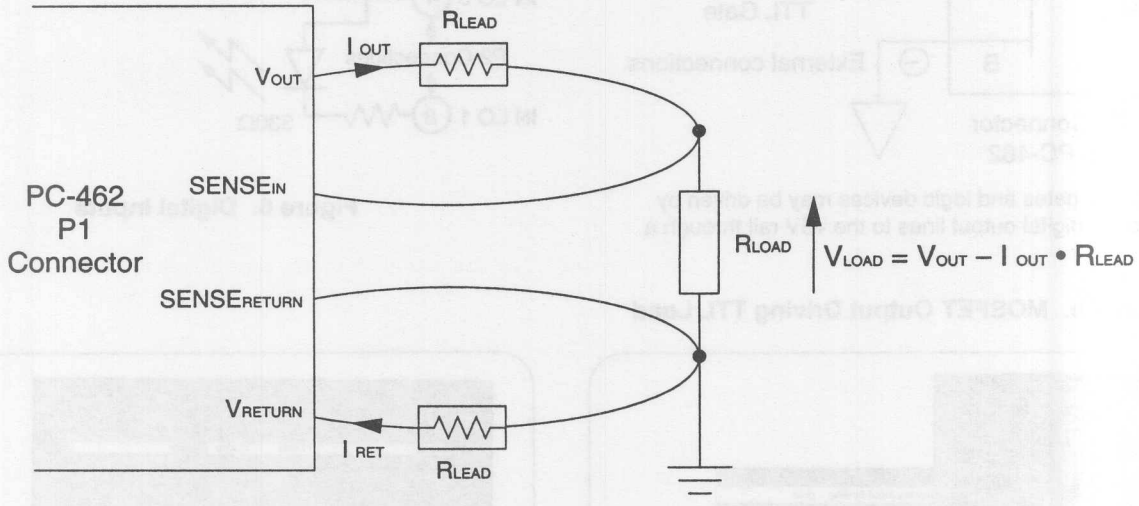
Figure 3. Isolated Digital Port - P2

P2 is a 9-pin, DB-9S connector and it provides connections to the digital I/O port.

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LOAD CONNECTIONS

Figure 2 illustrates a typical load connection to one of the output channels. Make sure that the SENSE OUT and SENSE RETURN connections are completed so that the voltage accross the load is exactly the required value. This remote voltage/current sensing facility eliminates attenuation errors due to lead resistance voltage drops. The feedback loop adapts the PC-462 output level so that the load voltage is regulated to the desired value, i.e. lead attenuation is cancelled. Note that there are no voltage drops on the SENSE IN or the V_{RET} lines since no current flows through them.



Important: Connect the sense outputs at the load.

Note: The voltage across the load is the true value. The voltage at the P1 connector (V_{OUT}) will be somewhat higher (±1V max.) to compensate for lead attenuation.

Figure 4. Typical Load Connections

MOSFET OUTPUT CONNECTIONS

The two isolated MOSFET output lines may be used to switch heavy loads or drive standard TTL level devices. Figure 5a illustrates a typical connection to a solid state relay. The relay in turn may switch higher rated loads - in excess of 300V, 100 millamps.

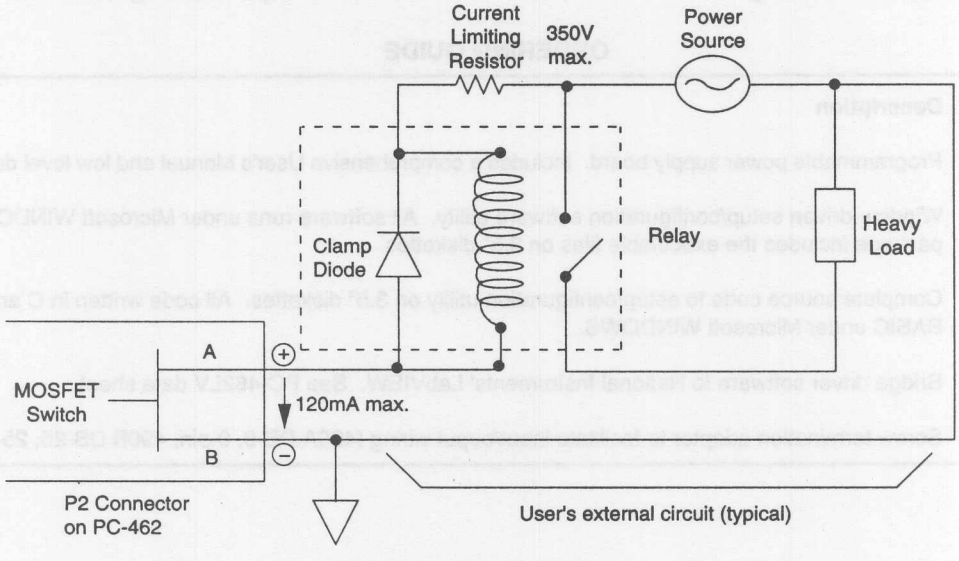
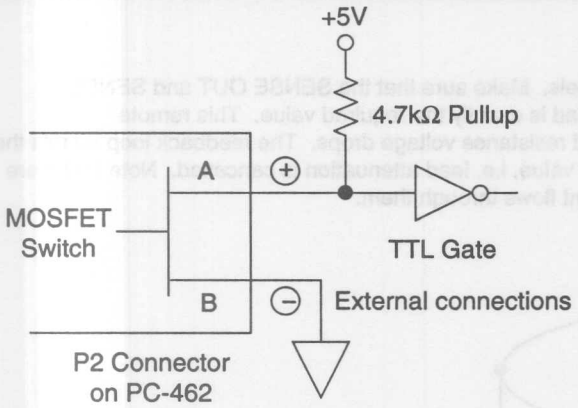


Figure 5a. Typical MOSFET Output Switching a Relay



Standard TTL gates and logic devices may be driven by pulling up the digital output lines to the +5V rail through a resistor.

Figure 5b. MOSFET Output Driving TTL Load

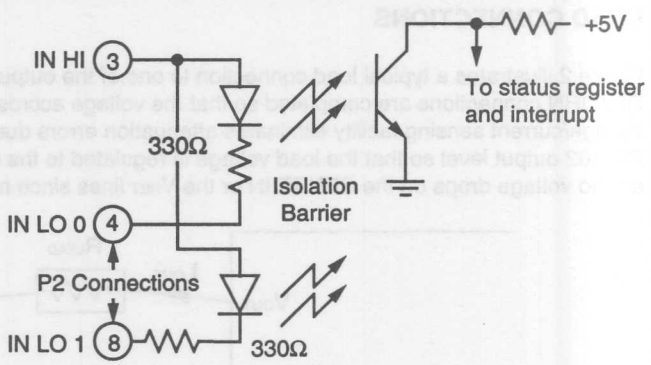


Figure 6. Digital Inputs

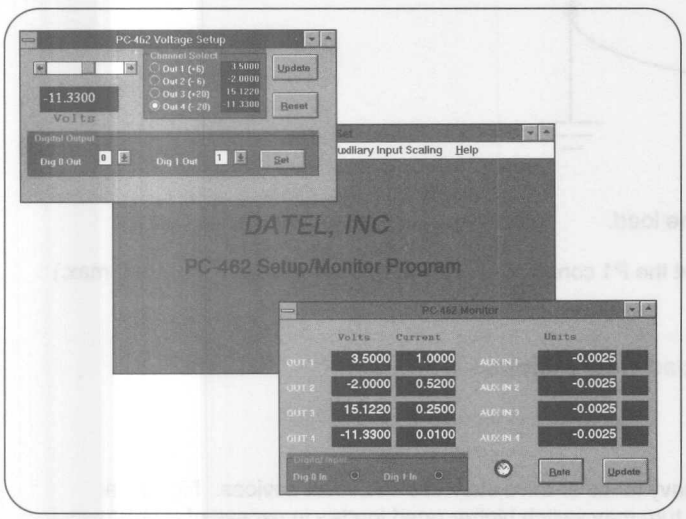


Figure 7. PC-462SET Channel Setup and Monitoring

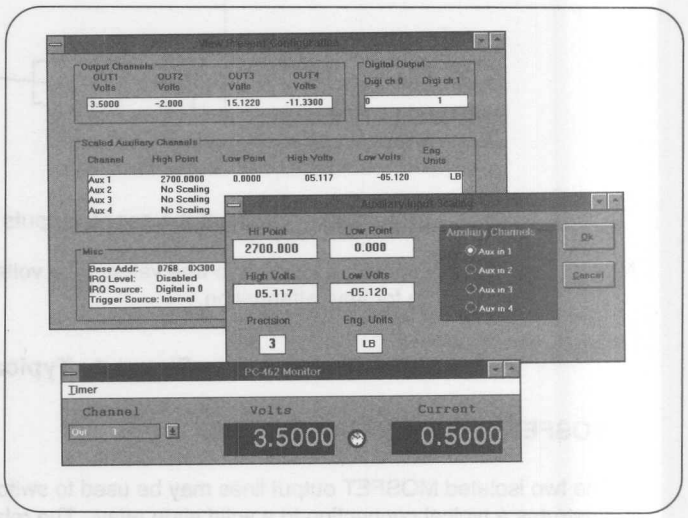


Figure 8. PC-462SET Configuration and Input Scaling Windows

ORDERING GUIDE

Model	Description
PC-462	Programmable power supply board. Includes a comprehensive User's Manual and low level driver library.
PC-462SET	Window-driven setup/configuration software utility. All software runs under Microsoft WINDOWS. This package includes the executable files on 3.5" diskettes.
PC-462SRC	Complete source code to setup/configuration utility on 3.5" diskettes. All code written in C and Visual BASIC under Microsoft WINDOWS.
PC-462LV/LVS	Bridge driver software to National Instruments' LabVIEW. See PC-462LV data sheet.
PC-490A/-490B	Screw termination adapter to facilitate input/ouput wiring (490A DB-9, 9-pin, 490B DB-25, 25-pin)

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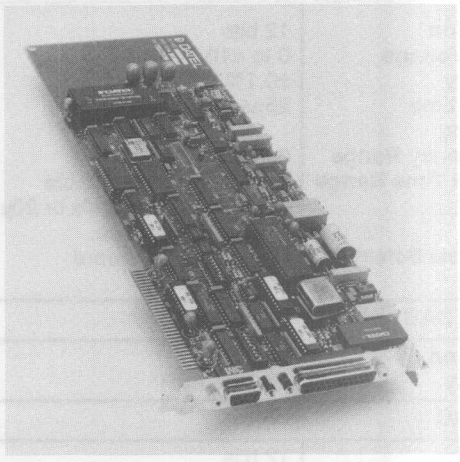
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PC-465
PC-Based, Electronic Load Controller Board

PRELIMINARY DATA SHEET

FEATURES

- **Fully programmable electronic load controller**
- **Part of a complete power supply test system when combined with DATEL's PC-EL and PC-467**
- **High-resolution current and voltage measurement**
- **Programmable dynamic loading up to 25kHz**
- **Full control over load amplitude, offset, period, and slew rate**
- **Safety monitoring of over-current and over-temperature load conditions**
- **Virtual instrument software package available**



GENERAL DESCRIPTION

DATEL's PC-465 is a fully programmable controller board for DATEL's PC-EL electronic load. In combination with the PC-EL, the PC-465 can easily generate almost any desired load condition. An on-board 12-bit A/D converter provides high-resolution current and voltage readings for basic power supply evaluaton. For more vigorous evaluation of power supply performance, DATEL's PC-467 may be added to create a complete power supply test and evaluation system.

Together with the PC-EL, the PC-465 offers complete load control. Besides basic open and short-circuit modes, the PC-465 offers programmable constant-current and resistive-load modes. Dynamic current conditions can also be generated by the PC-465. The current waveform amplitude, offset, duty cycle, period and slew rate are all fully programmable. Alternatively, an external waveform generator may be used to create other load conditions. All features are easily controlled by a Windows based software package, creating an easy-to-use "bench-top" virtual instrument right on your PC.

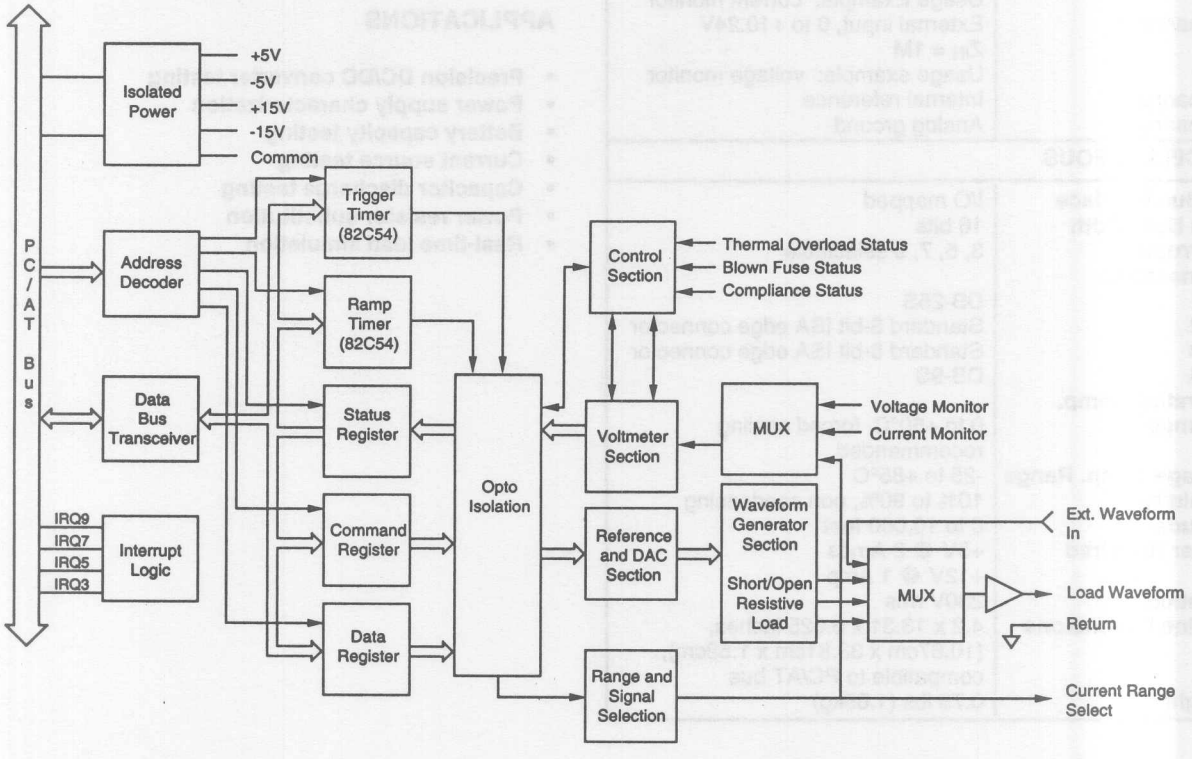


Figure 1. PC-465 Simplified Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C unless otherwise specified)

WAVEFORM DAC	
Resolution	12 bits
Output Voltage	0 to +10.24V
Accuracy	±0.1% FSR
Settling time	25µs to ±0.05% FSR
Operating Frequency Range	0.03Hz to 1kHz
Rise/Fall Time Range	Software programmable 250µs to 1.6 seconds or 20µs in square wave mode.
Duty Cycle Selection	1% to 100% software programmable
OFFSET DAC	
Resolution	12 bits
Accuracy	±0.05% FSR
GAIN DAC	
Resolution	12 bits
Accuracy	±0.05% FSR
RESISTOR DAC	
Resolution	12 bits
Polarity	Unipolar
Accuracy	±0.05% FSR
ANALOG INPUTS	
Resolution	12 bits + sign
Conversion Rate	2.5 conversions/second
Accuracy	±0.05% FSR ±2mV
Input channels:	4 single-ended
Channel 0	External input, 0 to +10.24V Z_{IN} = 1M Usage Example: current monitor
Channel 1	External input, 0 to +10.24V Z_{IN} = 1M Usage example: voltage monitor
Channel 2	Internal reference
Channel 3	Analog ground
MISCELLANEOUS	
PC Bus Interface	I/O mapped
Data Bus Width	16 bits
Interrupts	3, 5, 7, 9 selectable
Connectors:	
P1	DB-25S
P2	Standard 8-bit ISA edge connector
P3	Standard 8-bit ISA edge connector
P4	DB-9S
Operating Temp. Range	0 to +60°C, forced cooling recommended
Storage Temp. Range	-25 to +85°C
Humidity	10% to 90%, non condensing
Altitude	0 to 10,000 feet
Power Required	+5V @ 2 Amps +12V @ 1 Amp
Isolation	230V rms
Outline Dimensions	4.2 x 13.31 x 0.625 inches, (10.67cm x 33.81cm x 1.59cm), compatible to PC/AT bus
Weight	0.75 lbs (1.65kg)

OPERATION OVERVIEW

The PC-465 uses buffered 12-bit D/A converters to generate the control signals needed to operate the DATEL PC-EL electronic load. All features are controlled by on-board registers mapped into the host computer I/O space through the ISA bus. These registers provide control over all basic PC-EL load operation modes: resistive, constant/dynamic current, short circuit, and open circuit.

In the resistance mode, the PC-EL acts as an ideal resistor programmable to a wide range of values. In current mode, the PC-465 can produce both steady state and dynamic current load conditions. The PC-465 can easily generate both ramp and square-wave type current load waveforms. On-board registers, timers and control logic allow selection of all waveform characteristics. Once the mode and its parameters are selected, the performance of the power supply or other unit under test may be monitored by the on-board 12-bit A/D, yielding accurate voltage, and current readings.

Custom software can be easily written in any standard language: C, Basic, Pascal, etc., however, a complete software package is available that makes the PC-465/PC-EL as easy to operate as any bench-top instrument. Just connect the power supply under test to the PC-EL load and sense inputs, connect the PC-EL control port to the PC-465 and then run the optional virtual instrumentation software (PC-465WIN). Finally, select the desired parameters and collect your voltage and current readings.

APPLICATIONS

- **Precision DC/DC converter testing**
- **Power supply characterization**
- **Battery capacity testing**
- **Current source testing**
- **Capacitor discharge testing**
- **Power resistor substitution**
- **Real-time load simulation**

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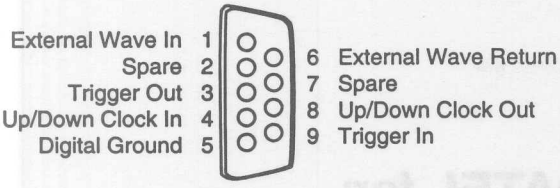


Figure 2. P4 Control Connector DB-9S

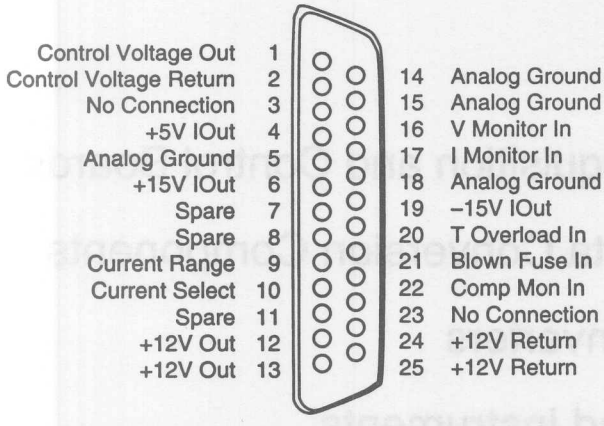


Figure 3. P1 Load Input Connector DB-25S

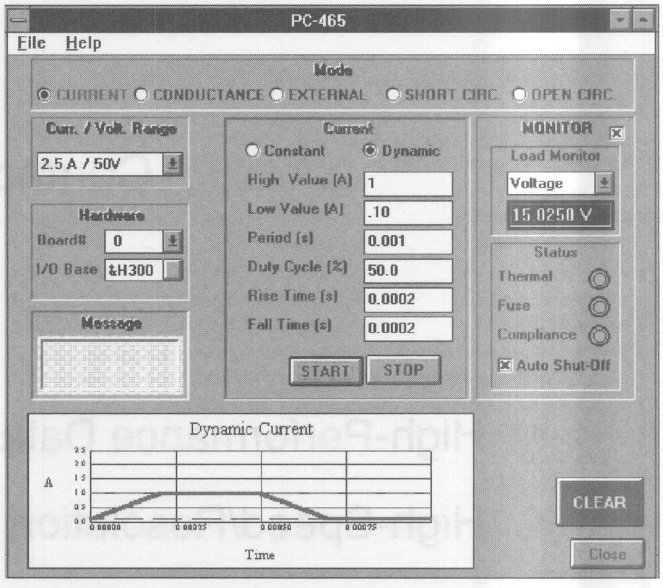


Figure 4. PC-465 Virtual Instrument Panel

ORDERING INFORMATION

Model	Description
PC-465	Electronic Load Controller Board
PC-465WIN	Windows setup/configuration program. Includes executable files on 3.5-inch, 1.44M.
PC-465WINS	Source code for PC-465WIN
PC-EL-25A/50V	0 to 25A (50V max.) Electronic Load - see PC-EL data sheet
PC-EL-10A/100V	0 to 10A (100V max.) Electronic Load
PC-EL-1A/500V	0 to 1A (500V max.) Electronic Load
PC-467	Power Supply Measurement Board - see PC-467 data sheet
PC-467WIN	Windows setup/configuration program. Includes executable files on 3.5-inch, 1.44M.
PC-467WINS	Source code for PC-467WIN
PC-467PWRSYS	Complete power supply test system software

Each board is power-cycle burned-in, tested, and calibrated. All models include a user's manual. The warranty period is one year.

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PC-EL Series
400 Watt Voltage-Controlled Electronic Load

PRELIMINARY DATA SHEET

FEATURES

- **Programmable electronic load module**
- **400 Watts maximum load capacity**
- **Parallel load capability for higher current and power applications**
- **Three models available in the following ranges:**
  - **0 to 25A (50V max.)**
  - **0 to 10A (100V max.)**
  - **0 to 1A (500V max.)**
- **Dynamic loading to 25kHz**
- **Constant current, constant resistance, and constant voltage operating modes using DATEL's PC-465**



GENERAL DESCRIPTION

The PC-EL Series of programmable electronic loads feature state-of-the-art design for testing DC power supplies. The Series offers three models with loading currents from 0.1 to 25 Amps full scale range and loading voltages of 50 to 500 Volts full scale range. Up to 400 Watts may be dissipated by using external heatsinking. The PC-EL functions as a voltage-controlled current sink. Its small size and simple interface make it ideal for power supply manufacturing, incoming inspection, and power component testing. The PC-EL can be combined with DATEL's PC/AT based PC-465 Electronic Load Controller Board and PC-467 Power Supply Measurement Board to create a powerful, low-cost power supply test system.

APPLICATIONS

- **Power supply test and characterization**
- **Battery capacity testing**
- **Current source testing**
- **Capacitor discharge testing**
- **Power resistor substitution**
- **Real-time load simulation**

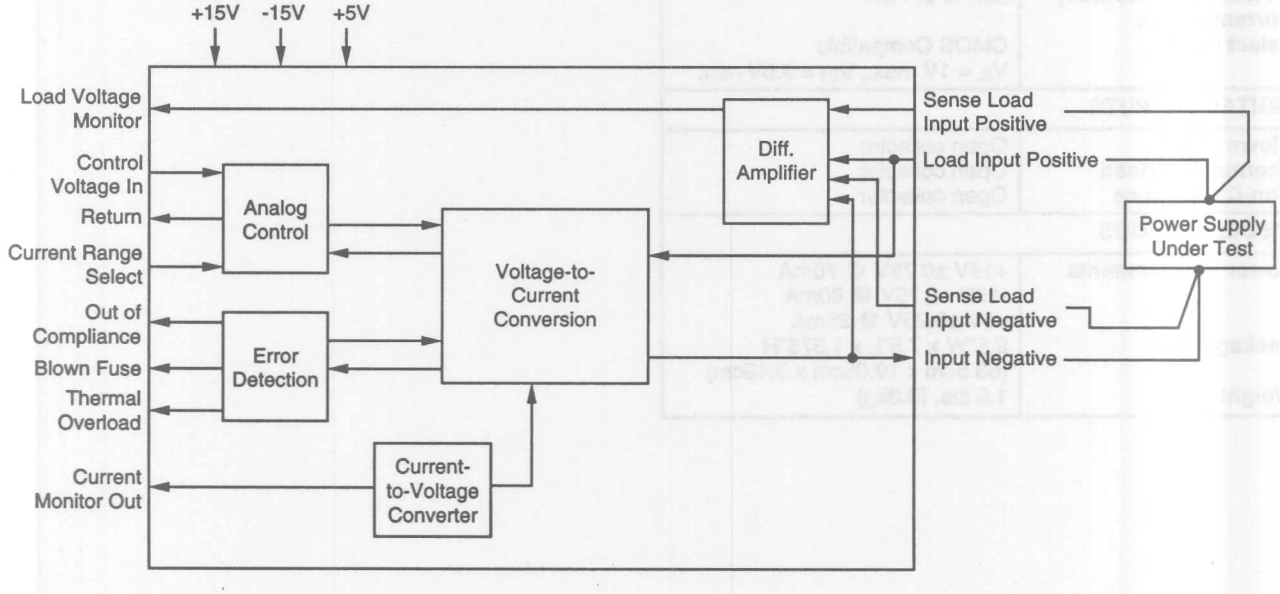


Figure 1. PC-EL Simplified Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C unless otherwise specified)

PERFORMANCE SPECIFICATIONS	
Loading Current (range selectable)	
PC-EL-1A/500V	0 to 1A or 0 to 0.1A
PC-EL-10A/100V	0 to 10A or 0 to 1A
PC-EL-25A/50V	0 to 25A or 0 to 2.5A
Current Resolution	±0.025%FSR
Accuracy	±0.1%FSR
Loading Voltage Compliance Range	
PC-EL-1A/500V	2 to 500V
PC-EL-10A/100V	2 to 100V
PC-EL-25A/50V	2 to 50V
Load Capacity	400W (see derating chart Fig. 4)
Control Voltage Input	0 to +10V
Control Voltage Input Impedance	1MΩ
Settling Time (full scale step input)	25µs
Temperature Coefficient	100ppm/°C
READBACK SPECIFICATIONS	
Load Current Readback Range (0 to +10V)	
PC-EL-1A/500V	0 to 1A or 0 to 0.1A
PC-EL-10A/100V	0 to 10A or 0 to 1A
PC-EL-25A/50V	0 to 25A or 0 to 2.5A
Load Current Readback Accuracy	±0.1% of FSR
Load Voltage Readback Range (0 to +10V)	
PC-EL-1A/500V	0 to 500V
PC-EL-10A/100V	0 to 100V
PC-EL-25A/50V	0 to 50V
Load Voltage Readback Accuracy	±0.1% of FSR
Current Range Select Input	CMOS Compatible V_{IL} = 1V max., V_{IH} = 3.5V min.
DIGITAL OUTPUTS	
Blown Fuse	Open collector
Thermal Overload	Open collector
Non-Compliance	Open collector
MISCELLANEOUS	
Power Requirements	+15V ±0.75V @ 70mA -15V ±0.75V @ 60mA +5V ±0.25V @ 25mA
Package Size	2.5"W x 7.5"L x 1.375"H (63.5cm x 19.05cm x 3.49cm)
Weight	1.5 lbs. (3.3kg)

OPERATION OVERVIEW

The PC-EL electronic load is a voltage-controlled current sink. An input control voltage of 0 Volts results in a 0 Ampere load current; a 10V control voltage results in a full scale load current. Two full scale current ranges are available for each model. The 1A/500V model has selectable ranges of 0 to 1A or 0 to 0.1A. The 10A/100V model offers 10A and 1A ranges. The 25A/50V model offers 25A and 2.5A ranges.

The PC-EL has built-in protection for over-current, over-temperature, and reverse load connection. The PC-EL also includes Load Sense inputs for accurate load voltage measurements. This compensates for voltage drops due to high currents flowing in the wires to the device under test (DUT) .

The PC-EL also contains a differential instrumentation amplifier which scales the load voltage into an output range of 0 to +10V. For example, in the PC-EL-10A/100V, the instrumentation amplifier scales the 100V to 10V.

The PC-EL packaging has been designed to allow for use with external heatsinking for high wattage applications.

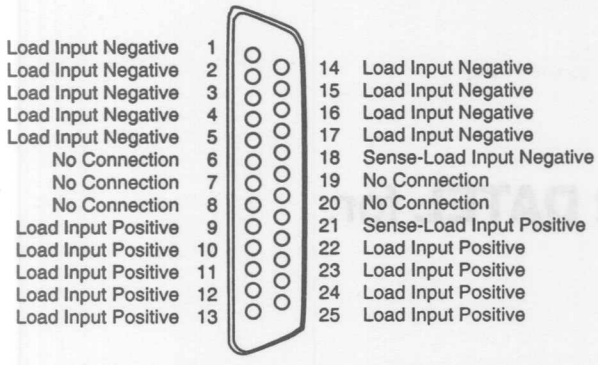


Figure 2. DB-25S Load Input Connector - P2

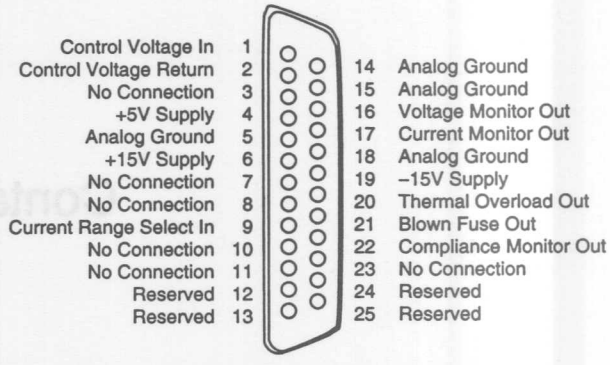


Figure 3. DB-25P Control Connector - P1

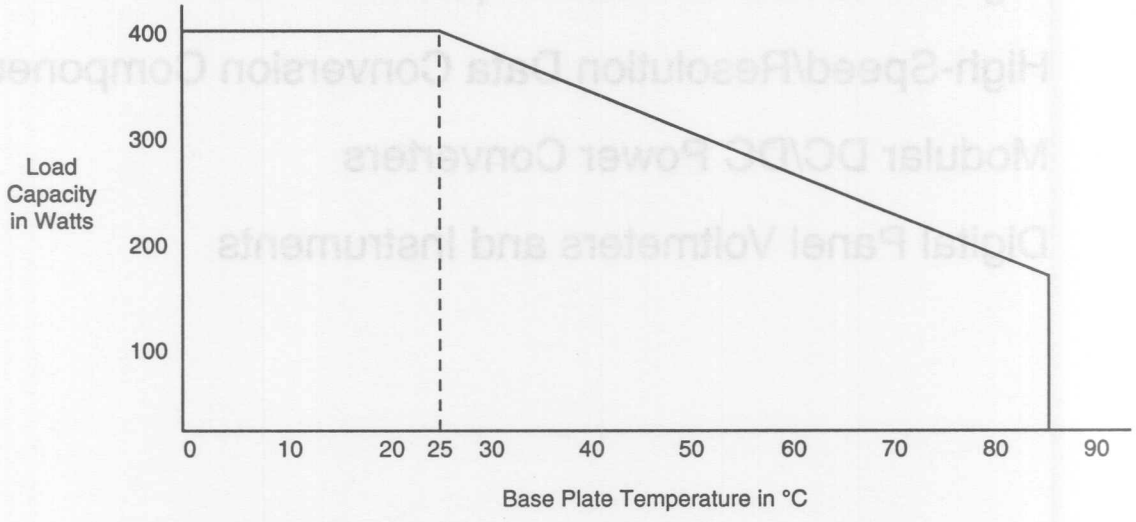


Figure 4. Load Capacity

ORDERING INFORMATION

Model	Description
PC-EL-25A/50V	0 to 25A (50V max.) Electronic Load
PC-EL-10A/100V	0 to 10A (100V max.) Electronic Load
PC-EL-1A/500V	0 to 1A (500V max.) Electronic Load
PC-465	Electronic Load Controller Board - see PC-465 data sheet.
PC-465WIN	Windows setup/configuration program. Includes executable files on 3.5-inch, 1.44M.
PC-465WINS	Source code for PC-465WIN
PC-467	Power Supply Measurement Board - see PC-467 data sheet.
PC-467WIN	Windows setup/configuration program. Includes executable files on 3.5-inch, 1.44M.
PC-467WINS	Source code for PC-467WIN
PC-467PWRSYS	Complete power supply test system software.

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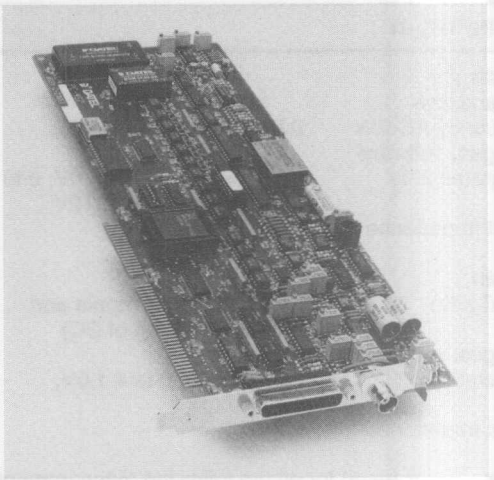
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PC-467
PC-Based, Power Supply Measurement Board

PRELIMINARY DATA SHEET

FEATURES

- **Use with PC-465 Electronic Load Controller Board and PC-EL Electronic Load to configure a complete power supply test station.**
- **Outstanding performance-price value**
- **Virtual instrument, Windows-based software**
- **Measure PARD, transient response, switching frequency, efficiency, and line/load regulation under dynamic load conditions**
- **Use in high-volume production testing, incoming inspection and product evaluation**



GENERAL DESCRIPTION

The PC-467, in conjunction with DATEL's PC-465 Electronic Load Controller Board and PC-EL Electronic Load, form a complete, easy-to-use, low-cost, PC-based power supply test system. The PC-467 exploits a combination of pure analog measurement techniques and high-speed, high-resolution A/D converters (for highly accurate digitized measurements) to record the instantaneous values of the input and output parameters of the power supply under test.

The PC-465/467 Power Supply Test Station functions as a virtual instrument with Windows compatible software. Routine performance tests include measuring input current and voltage, output current and voltage, line and load regulation, input and output ripple (amplitude and frequency), output noise spikes (Vp-p), transient response, input/output turn on/off characteristics, efficiency, current limiting, short circuit testing, etc. The user friendly, menu driven software allows easy data recording, manipulation, and display.

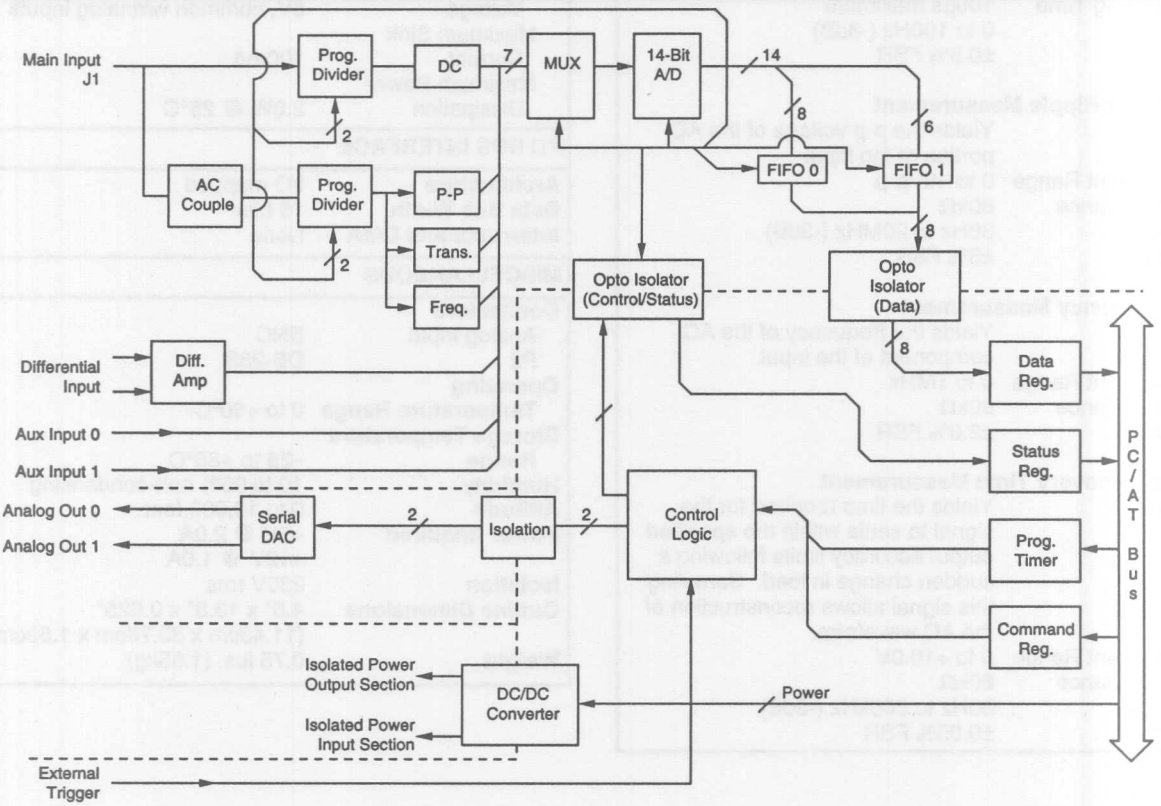


Figure 1. PC-467 Simplified Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C unless otherwise specified)

INPUT SPECIFICATIONS

MAIN INPUT, J1

DC Path

DC and low-frequency AC BW	0 to 100Hz, 25VAC max.
Ranges, software programmable	0 to +5.12V, 0 to +25.6V, 0 to +102.4V and 0 to +512V
Input Impedance	1MΩ

AC Path

Bandwidth	30Hz to 20MHz (ripple and transients on top of DC)
Ranges, software selectable	0 to +0.10V, 0 to + 1.0V, 0 to +10.0V
Input Impedance	80kΩ

A/D Converter (used for all the following measurements)

Resolution	14 bits
Input Range	0 to +10.0V
Maximum Conversion Rate	1 MSPS
FIFO Memory	1k samples

MEASUREMENT FUNCTIONS

DC Voltage Measurement

Description	Yields DC voltage level
Measurement Range	0 to +512V max.
Input Type	Single-ended, unipolar
Input Impedance	1MΩ
Input Settling Time	100µs maximum
Bandwidth	0 to 100Hz (-3dB)
Accuracy	±0.5% FSR

Peak-to-Peak Ripple Measurement

Description	Yields the p-p voltage of the AC portion of the input
Measurement Range	0 to 10Vp-p
Input Impedance	80kΩ
Bandwidth	30Hz to 20MHz (-3dB)
Accuracy	±5% FSR

Ripple Frequency Measurement

Description	Yields the frequency of the AC component of the input
Measurement Range	0 to 1MHz
Input Impedance	80kΩ
Accuracy	±2.0% FSR

Transient Recovery Time Measurement

Description	Yields the time required for the signal to settle within the specified output accuracy limits following a sudden change in load. Sampling this signal allows reconstruction of the AC waveform.
Measurement Range	0 to +10.0V
Input Impedance	80kΩ
Bandwidth	30Hz to 500kHz (-3dB)
Accuracy	±0.05% FSR

MAIN INPUT MEASUREMENTS

Peak-to-Peak DC Measurement

Description	Low-frequency AC measurements
Range	0 to +10.0V
Input Impedance	80kΩ
Bandwidth	0 to 100Hz (-3dB)
Accuracy	±5% FSR

AUXILIARY INPUTS, 0, 1, and DIFFERENTIAL INPUT

Auxiliary Input Range	0 to +5.12V
Differential Input Range (pins 2, 3 of P2)	0 to +0.512V
Differential Input Impedance	1GΩ/5pF
Common-mode Input Impedance	1GΩ/5pF
Accuracy	±0.25% FSR

ANALOG OUTPUTS

2 Channels, Isolated from the ISA bus and analog input

Output Range	0 to +5.00V
Maximum Current	5mA
D/A Resolution	12 bits
Maximum Update Rate	66.7kHz
Absolute Accuracy	±0.2% FSR of output, ±10mV

DIGITAL OUTPUTS

Parallel 8-bit, Isolated Digital Output Port

Output Driver	Open collector ULN2803 or equivalent
Maximum Pull-up Voltage	5V, common w/analog inputs
Maximum Sink Current	100mA
Maximum Power Dissipation	2.0W @ 25°C

PC BUS INTERFACE

Architecture	I/O mapped
Data Bus Width	16 bits
Interrupts and DMA	None

MISCELLANEOUS

Connectors	
Analog Input	BNC
P2	DB-25S
Operating Temperature Range	0 to +60°C
Storage Temperature Range	–25 to +85°C
Humidity	10 to 90% non-condensing
Altitude	0 to 10,000 feet
Power Required	+5V @ 2.0A +12V @ 1.0A
Isolation	230V rms
Outline Dimensions	4.5" x 13.3" x 0.625" (11.43cm x 33.78cm x 1.59cm)
Weight	0.75 lbs. (1.65kg)

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OPERATION OVERVIEW

The PC-467 contains an analog measurement pre-processing section, an isolated high-speed 14 bit A/D converter, two isolated analog outputs, and eight isolated digital outputs. All features of the PC-467 are controlled by on-board registers mapped into the I/O space of the host computer through the ISA bus. Together, all of the above features create a simple and effective tool for DC/DC converter and other power source evaluation and testing.

The main test input signal is fed into two paths, an AC path which allows analysis of voltages up to 10 VAC, and a DC path for low-frequency measurements up to 500V dc. The AC path also leads to several analog processing subsections that generate DC voltages corresponding to such quantities as input ripple frequency and peak-to-peak amplitude.

In addition to the main input, two auxiliary inputs (5.12V) and one differential input (0.512V) are also available for measurement of additional external voltages. Selection of any of the above direct or pre-processed signals for A/D measurement is made through a software controlled multiplexer. A/D conversions may be initiated by software control or through an external trigger input. Parameters such as sampling rate and samples per trigger are also fully programmable and data from the A/D is buffered by a 1024 sample FIFO memory.

For added convenience, eight software controlled isolated digital outputs are also available for optional test fixture setup and control. Additionally, two isolated D/A's are provided for controlling relays or voltage programmable power supplies.

Obtaining a measurement is simple: set up your test fixture using the digital outputs, select the test signal type by setting the A/D input multiplexer, set the A/D sampling rate and sample count, wait for the FIFO to fill, and then read the data from the FIFO data register.

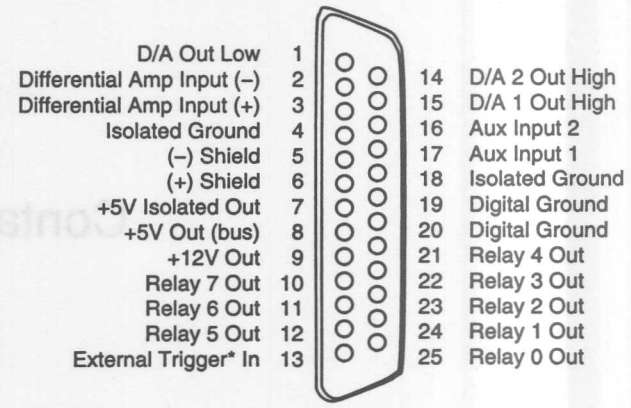


Figure 2. P2, DB-25S

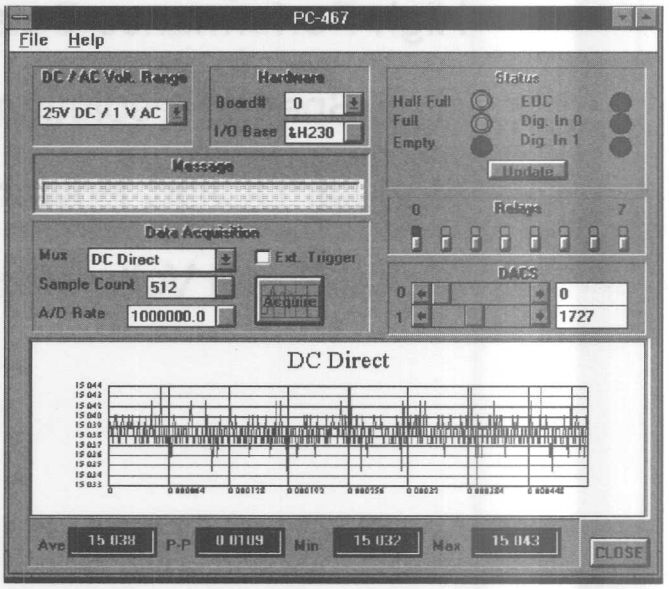


Figure 3. PC-467 Virtual Instrument Panel

ORDERING INFORMATION

Model	Description
PC-467	Power Supply Measurement Board
PC-467WIN	Windows setup/configuration program. Includes executable files on 3.5-inch, 1.44M.
PC-467WINS	Source code for PC-467WIN
PC-465	Electronic Load Controller Board - see PC-465 data sheet
PC-465WIN	Windows setup/configuration program. Includes executable files on 3.5-inch, 1.44M.
PC-465WINS	Source code for PC-465WIN
PC-EL-25A/50V	0 to 25A (50V max.) Electronic Load - see PC-EL data sheet
PC-EL-10A/100V	0 to 10A (100V max.) Electronic Load
PC-EL-1A/500V	0 to 1A (500V max.) Electronic Load
PC-467PWRSYS	Complete power supply test system software

Each board is power-cycle burned-in, tested, and calibrated. All models include a user's manual. The warranty period is one year.

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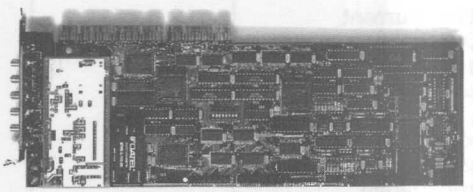
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Preliminary

PCI-416 Family
Ultra-Performance, Analog Input Boards for PCI Computers

FEATURES

- **The ideal array-processor "front end"**
- **Up to 10MHz A/D sampling rates**
- **Choice of 12 or 14-bit A/D resolutions**
- **Wideband inputs with low harmonic distortion**
- **Quick, 32-bit, PCI block transfers**
- **2 to 16-channel simultaneous sampling eliminates phase skew**
- **On-board A/D FIFO memory to 8k samples**
- **32 megasamples or greater data streaming**
- **Pre/post-trigger, gap-free, ring buffering**
- **Great for DSP, FFT's, digital filtering, etc.**
- **Compatible with Pentium®**



GENERAL DESCRIPTION

The PCI-416 Family consists of 9 advanced-performance, data acquisition boards based on the 32-bit PCI bus architecture. With an emphasis on continuous, non-stop, high-speed streaming of A/D samples to host memory or disk, the system has been optimized for a wide range of signal-processing and data-recording applications. In very long "baseline" studies or high-speed transient analysis, the PCI-416 can collect more than 64 megabytes of "seamless" digitized data to host memory.

Typical PCI transfers are made at 16 megasamples per second in DMA bursts. Exploiting a unique "banked" FIFO architecture, the PCI-416 moves two A/D words in each 32-bit PCI transfer. The FIFO memory (up to 8k samples deep) serves to decouple the precise timing of the A/D converter from the block bursts of the PCI bus.

The PCI-416's optional analog front-ends all utilize DATEL's low-noise, wide-bandwidth A/D converters. All models exhibit excellent harmonic distortion and perform well in DSP/FFT applications. Our PCI-416SET software readily implements a menu-driven, "no-programming", fast data recording system to memory and disk.

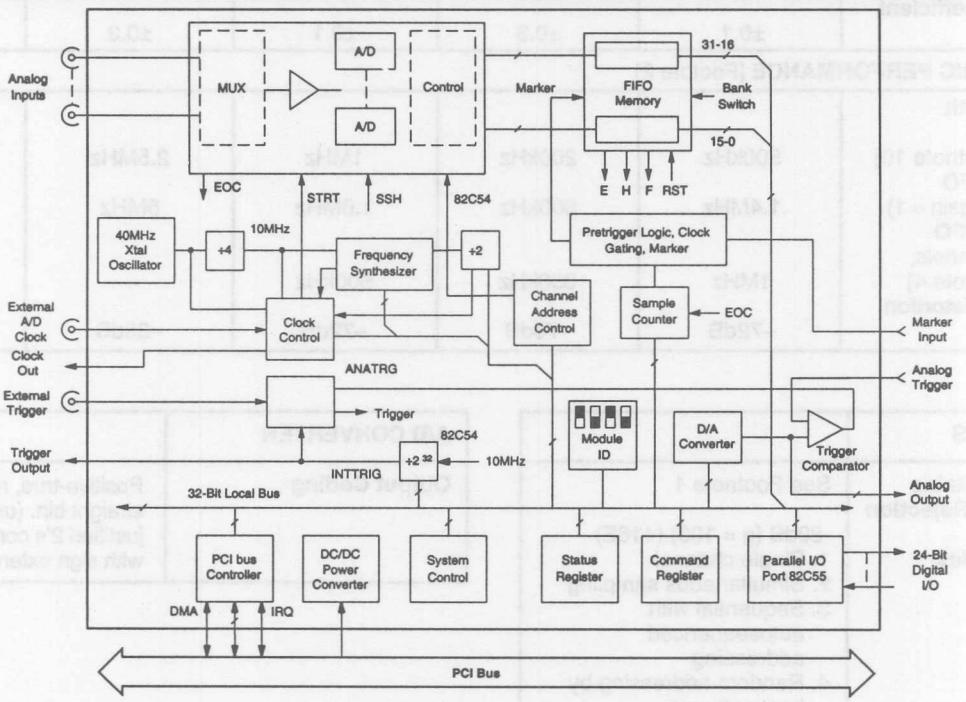


Figure 1. PCI-416 Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	PCI-416A	PCI-416B	PCI-416C	PCI-416D	PCI-416E
Number of Channels	4 Simultaneous	4	4	1	16SE/8D
Input Configuration (non-isolated)	Single Ended	Single Ended	Single Ended	Differential	SE or Diff.
Full Scale Input Ranges (user-selectable) (gain = 1)	0 to +10V ±10V [Footnote 1]	0 to +10V ±10V ±5V	0 to +10V ±10V ±5V	±5V	0 to +10V ±10V ±5V [Footnote 1]
Input Bias Current	±1nA	±1nA	±1nA	—	±1nA
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	2µs	2µs	2µs
Common Mode Voltage Range, maximum	—	—	—	±1V	±10V
Input Impedance [Footnotes 6 and 9]	10MΩ	10MΩ	10MΩ	2kΩ	100MΩ
SAMPLE/HOLD					
Acquisition Time (FSR step to 0.01% of FSR, max.)	900ns	750ns	200ns	50ns	750ns
Aperture Delay	15ns	20ns	20ns	10ns	20ns
Aperture Delay Uncertainty	±8ps	±100ps	±40ps	±7ps	±40ps
A/D CONVERTER					
Resolution	12 bits	14 bits	12 bits	12 bits	12 bits
Conversion Period	500ns	1.6µs	500ns	200ns	500ns
SYSTEM DC CHARACTERISTICS [Footnote 7]					
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1	±2	±1
Differential Non-linearity (LSB of FSR)	±0.75	±1	±0.75	±1	±0.75
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.1	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.3	±0.1
SYSTEM DYNAMIC PERFORMANCE [Footote 2]					
System Bandwidth (single channel, FSR input) [Footnote 10]	500kHz	200kHz	1MHz	2.5MHz	200kHz
Throughput to FIFO (single channel, gain = 1)	1.4MHz	500kHz	1.6MHz	5MHz	2MHz
Throughput to FIFO (sequential channels, gain = 1) [Footnote 4]	1MHz	330kHz	500kHz	—	500kHz
Total Harmonic Distortion [Footnote 3]	–72dB	–75dB	–72dB	–68dB	–72dB

ANALOG INPUTS	
Programmable Gains	See Footnote 1
Common Mode Rejection (DC - 60Hz)	-80dB (g = 100) (416E)
Addressing Modes	1. Single channel 2. Simultaneous sampling 3. Sequential with autosequenced addressing 4. Random addressing by host software

A/D CONVERTER	
Output Coding	Positive-true, right-justified, straight bin. (unipolar) or right-justified 2's comp. (bipolar) with sign extension thru bit 15

FUNCTIONAL SPECIFICATIONS CONTINUED

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	PCI-416F	PCI-416G	PCI-416H	PCI-416J
Number of Channels	2 Simultaneous	2 Simultaneous	1	8 Simultaneous
Input Configuration (non-isolated)	Single Ended	Single Ended	Differential	Single Ended
Full Scale Input Ranges (user-selectable) (gain = 1)	0 to +10V ±5V	±5V or 0 to +10V (separate models)	±5V (other ranges special order)	0 to +2.5V ±5V, ±10V [13] (separate unipolar & bipolar models)
Input Bias Current	±1nA	±1nA	—	±50nA (unipolar version)
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	1µs	—
Common Mode Voltage Range, maximum	—	—	±1V	—
Input Impedance [Footnotes 6 and 9]	1kΩ	1MΩ	2kΩ	8kΩ (bipolar)
SAMPLE/HOLD				
Acquisition Time (FSR step to 0.01% of FSR, max.)	165ns	350ns	35ns	400ns
Aperture Delay	20ns	20ns	±10ns	—
Aperture Delay Uncertainty	±40ps	±70ps	3ps rms	—
A/D CONVERTER				
Resolution	12 bits	14 bits	12 bits	12 bits
Conversion Period	400ns	500ns*	100ns	2µs (all chans. in simul. sampling)
SYSTEM DC CHARACTERISTICS [Footnote 7]				
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1.5	±1 max.
Differential Non-linearity (LSB of FSR)	±1	±1	±1	±1 max.
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 13]
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 13]
SYSTEM DYNAMIC PERFORMANCE [Footnote 2]				
System Bandwidth (single channel, FSR input) [Footnote 10]	1MHz	500kHz	5MHz	100kHz
Throughput to FIFO (single channel, gain = 1)	2MHz	1MHz*	10MHz	400kHz
Throughput to FIFO (sequential channels, gain = 1) [Footnote 4]	2MHz/chan. (2 chans.)	1MHz/chan.* (2 chans.)	—	2MHz (250kHz/chan. 8 chans. simul.)
Total Harmonic Distortion [Footnote 3]	–70dB	–80dB	–65dB	–77dB

*Dual 2MHz 14-bit sampling is available on special order.

SPECIFICATIONS, CONTINUED

(Typical @ +25°C, dynamic conditions, unless noted)

A/D SAMPLE CLOCK	
Sample Clock Sources	Selectable from among: 1. Frequency synthesizer 2. 10MHz crystal oscillator 3. 20MHz crystal oscillator 4. 16-stage binary divider to either 1 or 2, maximum input: 10MHz 5. External digital input
Frequency Synthesizer	Output 5-10MHz in 625Hz steps, further divisible by 16-stage binary divider, all software programmable. Up to 40MHz is available in 2500Hz steps.
Total Sample Range	76.3Hz to 10MHz (40MHz avail.)
Oscillator Frequency Accuracy	±50ppm (+20 to +30°C)
Crystal Aging	±5ppm/year
TRIGGER CONTROL	
Trigger Sources [Footnote 11]	1. Analog threshold comparator using internal D/A to set trip level 2. Internal trigger derived from10MHz timebase, divided by 32-stage divider (82C54). Range: 20ns to 429.5 seconds. 3. External digital trigger
Trigger Response	Selectable from among: 1. Starts one frame ("single trigger mode") 2. Collects repeating frames, each started by a trigger ("continuous trigger mode"), gatable while trigger remains asserted. 3. Runs the A/D "forever" (sample counter disabled)
A/D Samples per Frame	1 to 16,777,216 samples (24-bit counter) or "forever"
Analog Trigger Input Range	±10V
Analog Trigger Response	2µs [Footnote 5]
Analog Trigger Hysteresis	±40mV
Marker	Digital input which sets A/D bit 15 to logic "1" for one A/D clock cycle. Used to tag samples to external events if enabled.
Pretrigger	The sample down-counter is delayed until an external trigger. Pretrigger samples are stored in a host ring buffer for transient capture, if enabled.

ANALOG OUTPUT	
Number of Channels	One channel
Function	Selectable from among: 1. General purpose analog output 2. Threshold comparator for A/D trigger
Resolution	12 bits
Output Voltage Range	0 to +10V, ±5V, ±10V at 5mA max. (user selectable)
Linearity	±0.05% of FSR
Settling Time	5 microseconds (10V step)
Input Coding	Straight binary
PCI Bus	
Data Bus Size	32 bits
Address Bus Size	32 bits
PCI Controller Type	AMCC S5933 bus master mode
Spec. Conformance	PCI revision 2.0
Data Transfer	32-bit I/O or DMA
Direct Memory Access	One channel, selectable by software on channels 3, 5, 6, or 7. Terminal count appears as local status bit or PCI interrupt.
Interrupts	One interrupt, software selectable on level 10, 11, 12, or 15
Interrupt Sources	FIFO, half full sample count reached (ACQuire flag), DMA terminal count from bus
MISCELLANEOUS	
	preset to identify A/D module type. May be changed if another module is used.
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain per channel for SSH on PCI-416A,F,G. A single offset and gain pot is provided on PCI-416B,C,D,E. Recommended recalibration interval is 90 days in stable conditions.
Operating Temp. Range	0 to +60°C
Storage Temp. Range	–25 to +85°C
Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet, forced cooling is recommended
Power Required	+5V dc @ 3.0A max. from PCI bus
Outline Dimensions	4.2 x 12.28 x 0.5 inches, compatible to PCI bus
A/D MEMORY	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024 or 8192 A/D samples (other sizes on special order)

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CONNECTORS	
PCI bus	120-pin (dual 60) PCI edgeboard connector
Analog Input (4 channels or less)	Four SMA miniature threaded coaxial, mounted on rear slot plate
Analog Input [Footnote 8] (more than 4 channels)	DB-25 25-pin connector mounted on rear plate
External Trigger [Footnote 12]	SMA miniature threaded coaxial on rear plate
External A/D Clock In	SMA miniature threaded coaxial on rear plate
Digital I/O Port	Internal header connector. External clock, D/A mounted on board interior, suitable for flat cables.
DIGITAL I/O PORT	
Configuration	24 lines, programmable as input or output with latches and handshakes
Controller	82C55
Levels	TTL logic, 1 TTL load in or out (direct from 82C55)
Outport Settling Time	50ns, after write operation

FOOTNOTES

1. Resistor-programmed gain from X1 to X100 is available on PCI-416E with increased settling delay at higher gains. Fixed gains of X1 and X10 on 2 channels, offering 1V ranges, are selectable on the PCI-416A.
2. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion, and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.
3. THD test conditions are:
   1. Input freq. 500kHz (416A,F) 200kHz (416B,E) 300kHz (416C) 1MHz (416D) 100kHz (416G) 2MHz (416H)
   2. Generator/filter THD is -90dB minimum.
   3. THD computed by FFT to 5th harmonic.

$$THD = 20\left(\log 10 \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}\right)$$

   4. Inputs are full scale –0.5dB. No channel advance.
   5. A/D trigger rate = 1.5MHz (416A), 500kHz (416B,C,E), 4MHz (416D), 2MHz (416F), 1MHz (416G), 10MHz (416H).
4. The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the PCI-416C were scanned, the maximum sample rate on any one channel would be 2µs X 4 channels = 8µs (125kHz per channel).
5. For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10V.
6. The input impedance of 10MΩ minimum avoids attenuation errors from external source resistance. For many applications, an in-line coaxial 50 Ohm shunt, inserted adjacent to the front connectors, is recommended to reduce reflections and standing wave errors.
7. Allow 20 minutes warmup time to rated specifications for models PCI-416B,G.
8. A 25-pin DB-25S connector is used for the PCI-416E,J.
9. Input impedance is shown with power on. Impedance with power off is 1500 Ohms or less.
10. Full power bandwidth is shown at approximately 3% distortion level. This is not the –3dB amplitude response which is at a higher but non-Nyquist frequency.
11. Avoid mixing external triggers which are a close submultiple of the internal A/D start clock to prevent lost samples.
12. The 5th SMA connector may be rewired to either external trigger or external A/D clock.
13. PCI-416J bipolar input is user-selectable ±5V or ±10V per channel (default). Unipolar model is 0 to +2.5V. Total gain error over temperature range is ±4 LSB maximum. Total zero/offset error over temperature range is ±4 LSB maximum. Monotonicity: no missing codes over temperature range.

ORDERING INFORMATION

PCI-416 ____ ____ ____

Input Channels, A/D Resolution

A = 4SE simul. chans., 12 bits	F = 2SE simul. chans., 12 bits
B = 4SE chans., 14 bits	G = 2SE simul. chans., 14 bits
C = 4SE chans., 12 bits	H = 1D chan., 12 bits
D = 1D chan., 12 bits	J = 8SE simul. chans., 12 bits
E = 16SE/8D chans., 12 bits	

FIFO Memory Size

1 = 1k A/D samples
2 = 8k A/D samples (other sizes on special order)

A/D Input Polarity

A = Bipolar
B = Unipolar
Use this designator *only* for G and J models requiring polarity selection.

61-7342340	SMA male to BNC male coaxial cable, 1 meter length. One cable required per channel.
PC-490B	DB-25 screw termination adapter, 25-pin for PCI-416E,J.

Each board is power-cycle burned-in, tested, and calibrated. All models include a user's manual. A low-level "C" library source disk is available on request at no charge.

Software:

PCI-416SET	Setup/configuration data collection program. Executables only.
PCI-416SRC	Source code for setup and configuration program on MS-DOS disks. Includes "C" and assembly source code. Documentation is on disk.

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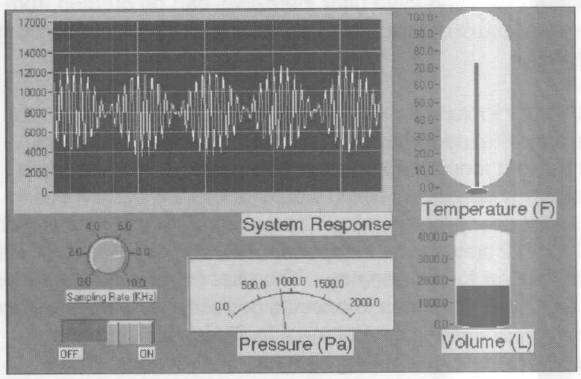
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PC-412LV

LabVIEW® Virtual Instrument Software for PC-411/412 Multifunction I/O Boards

FEATURES

- **Supports DATEL's PC-411/412 multifunction I/O boards**
- **Runs under Microsoft Windows®, uses Dynamic Data Exchange for interprocess communications**
- **Adaptable to all LabVIEW applications**
- **Easy-to-use visual programming environment**
- **Eliminates low level software development**
- **Interactive, customizable front panel controls**
- **Integrates data acquisition, processing, display, and storage in real time**
- **Supports all analog output and digital I/O functions**



GENERAL DESCRIPTION

National Instruments' LabVIEW transforms the PC-411/412 multifunction I/O boards into easy-to-use virtual instruments (VI's) that acquire, analyze, display, store, and generate analog and digital signals in real time. Low level software development is replaced by an intuitive visual programming system that harnesses all the power of Microsoft Windows - graphic user interface (GUI), access to more host memory, multi-tasking, and inter-process communications. Applications include process monitoring, laboratory automation, control, automatic test, manufacturing, education, and research.

The PC-411 is an analog input board for IBM-PC, PC/XT, PC/AT, and compatible computers that accepts 16 single-ended or 8 differential input signals and digitizes them up to 12 or 14-bit resolution. In addition to these analog inputs model PC-412 includes four analog output channels with simultaneous update and 12-bit resolution. Both models offer 8 digital inputs and 8 digital outputs for external logic devices.

LabVIEW's feature-rich program development system combined with DATEL's library of VI functions for the PC-411/412 provide the essential building blocks to create any conceivable LabVIEW application. Access to expanded and virtual memory means that more comprehensive application programs can be developed and larger amounts of A/D data can be collected and analyzed. Data and results can be passed using Dynamic Data Exchange (DDE) to other Windows tasks that are running simultaneously.

Graphical programming works like a flowchart - when the flowchart is complete, the program is done. PC-412LV creates a library of fast, simple, highly modular VI functions for the PC-411/412 that do not sacrifice board performance. The user builds VI's to configure the data acquisition hardware, process the data, and ultimately display and store that data without writing programs. Similar VI's can be created to update the analog output channels and to read and write the digital I/O ports. All VI's are assembled graphically using a mouse and can be edited at any time to modify functionality or appearance.

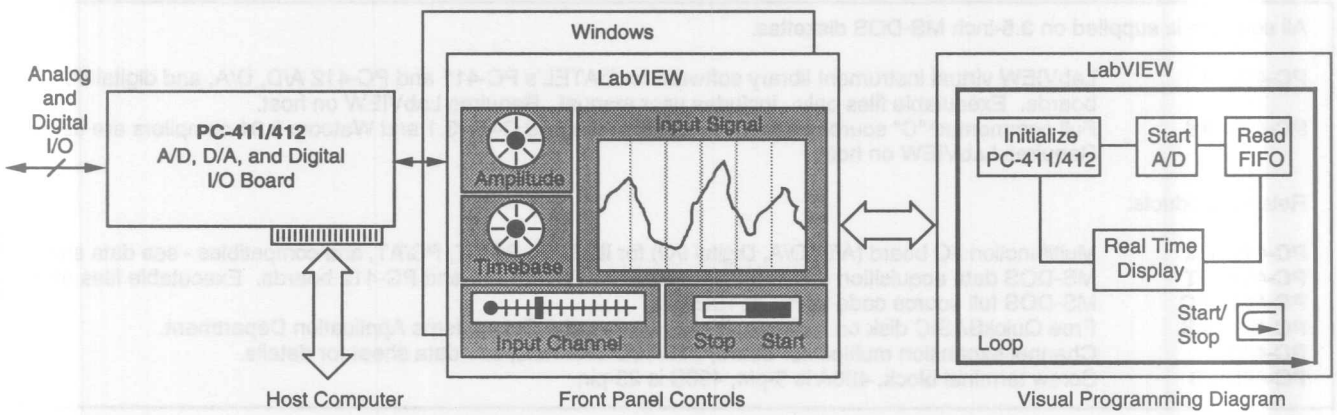


Figure 1. PC-412LV LabVIEW System Diagram

LabVIEW is a National Instruments trademark
IBM-PC is an IBM Corp. trademark
Windows is a Microsoft Corp. trademark

PC-412LV offloads as much programming as possible into the LabVIEW environment so the user has maximum control. Non-stop, seamless data acquisition continues on the PC-411/412 while LabVIEW simultaneously maintains the GUI and handles the A/D data stream in real time. Easily customized, interactive user interfaces can be created from the vast library of front panel controls and displays offered by LabVIEW.

PC-412LV includes extensive Dynamic Linked Library (DLL) functions that perform the PC-411/412 low level hardware control and monitor operations transparently. The software avoids any conditions which would lockup the system due to incorrect user programming. It provides VI functions that poll PC-11/412 status flags independent of, and simultaneous with, data transfer to host memory. The user stays in control as long as LabVIEW continues to execute correctly. The multi-window, visual programming environment facilitates building and accessing hierarchical VI programs. Multi-tasking allows context switches to other concurrent Windows applications without disrupting PC-411/412 operation or control.

The system optimizes two concurrent processes - PC-411/412 data acquisition while LabVIEW further processes or stores the uploaded data stream. The entire PC-411/412-LabVIEW combination uses only a few VI functions that are easy to understand and incorporate into a "block diagram" program. The basic concept is to initialize the PC-411/412 hardware, reset the FIFO A/D memory, monitor the FIFO and data acquisition flags, and upload blocks of data to LabVIEW memory buffers on the host. These data blocks can then be further processed as screen displays, indicators, graphs, sent to printers or plotters, or simply archived to disk file for later analysis. The A/D continues running and no data will be lost as long as LabVIEW uploads the A/D data faster than the data is being acquired.

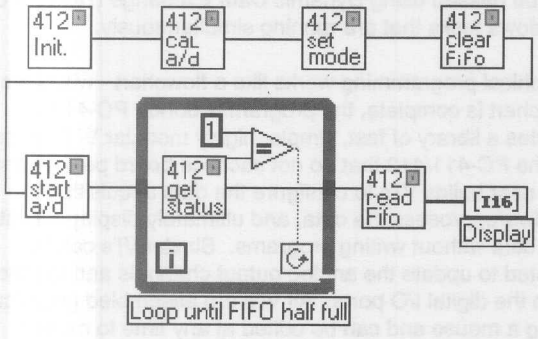


Figure 2. PC-412LV Visual Program

Virtual Instrument Library

In summary, PC-412LV includes the following VI functions:

PC-411/412 Initialize	Initialize the PC-411/412 hardware - model, I/O base address, FIFO size, input voltage range, and single-ended/differential input configurations.
A/D Calibration	A/D self-calibration procedure.
Write DAC's	Update the analog output channels - single channel or simultaneously.
Inport/Outport	Read/write 8-bit digital words from/to the digital input/output port.
Operating Mode	Specify A/D trigger source, trigger rate, sample rate, input channel, sample block length.
Clear FIFO	Reset/clear the contents of the FIFO.
Read FIFO	Read a block of A/D data from the FIFO on the PC-411/412 and fill a LabVIEW buffer.
Start/Stop A/D	Enable and disable the A/D.
Read Status	Read hardware status flags - FIFO empty/half full/full flags and data acquisition done flag.
Demultiplex Buffers	Unravel a multi-channel data buffer and extract data from one channel only - similar to decimation except only one channel is extracted.
PC-411/412 Demo	Complete data acquisition demonstration VI, including real time signal display.

ORDERING GUIDE

All software is supplied on 3.5-inch MS-DOS diskettes.

PC-412LV	LabVIEW virtual instrument library software for DATEL's PC-411 and PC-412 A/D, D/A, and digital I/O boards. Executable files only. Includes user manual. Requires LabVIEW on host.
PC-412LVS	Full commented "C" source code to PC-411LV. Borland C++ v3.1 and Watcom 9.01 compilers are used. Requires LabVIEW on host.

Related products:

PC-411/412	Multifunction I/O board (A/D, D/A, Digital I/O) for IBM-PC, PC/XT, PC/AT, and compatibles - see data sheet.
PC-411SET	MS-DOS data acquisition and control software for the PC-411 and PC-412 boards. Executable files only.
PC-411SRC	MS-DOS full source code to PC-411SET.
PC-411BAS	Free QuickBASIC disk on request. Please contact the Subsystems Application Department.
PC-440	Channel expansion multiplexer board, 32S/16D channels, see data sheet for details.
PC-490A/B	Screw terminal block, 490A is 9-pin, 490B is 25-pin.

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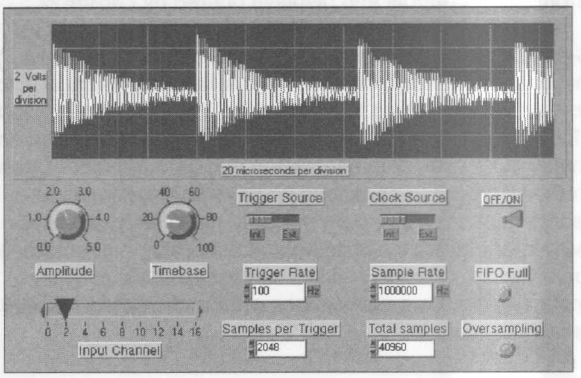
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PC-414LV

LabVIEW® Virtual Instrument Software for PC-414 Analog Input Boards

FEATURES

- **Supports DATEL's PC-414 family of high-speed analog input boards**
- **Runs under Microsoft Windows®, uses Dynamic Data Exchange (DDE)**
- **Adaptable to all LabVIEW applications**
- **Easy-to-use visual programming eliminates low level software**
- **Interactive, customizable front panel controls**
- **Integrates data acquisition, processing, display, and storage**
- **A/D sampling rates to 10MHz**
- **Optional multi-channel simultaneous sampling**



GENERAL DESCRIPTION

National Instruments' LabVIEW transforms the PC-414 family of high speed analog input boards into easy-to-use virtual instruments (VI's) that acquire, analyze, display, and store analog signals in real time. Low level software development is replaced by an intuitive visual programming system that harnesses all the power of Microsoft Windows - graphic user interface (GUI), access to more host memory (16 megabytes), multi-tasking, and inter-process communications using DDE. Applications include highly concurrent system testing, process monitoring and control, telemetry, radar, sonar, acoustics, DSP front end quantizer, education, and research.

The PC-414 is a family of ultra high speed, multi-channel analog input boards for the IBM-PC/AT, EISA, and compatible computers with sampling rates to 10MHz and A/D resolution to 12 and 14 bits. Phase correction and de-skewing of multi-channel signals is possible using the simultaneous sample/hold models. Local dual-ported First-In-First-Out (FIFO) memory supports data block transfers and "seamless" acquisition of very wide-bandwidth signals. Data can be streamed to third party remote receiver boards over a high speed DT-Connect I® compatible output port. The PC-414 also includes analog output and digital input/output (I/O) functions. LabVIEW's feature-rich program development system combined with DATEL's library of VI functions for the PC-414 provide the essential building blocks to create any conceivable LabVIEW application.

Graphical programming works like a flowchart - when the flowchart is accurate and complete, the program is done. PC-414LV offloads as much programming as possible into the LabVIEW environment so the user has maximum control. It creates a library of fast, simple, highly modular VI functions for the PC-414 that do not sacrifice board performance. The user builds VI's to configure the data acquisition hardware, process the data, and ultimately display and store that data without writing programs. Similar VI's can be created to update the analog output and to read and write the digital I/O port.

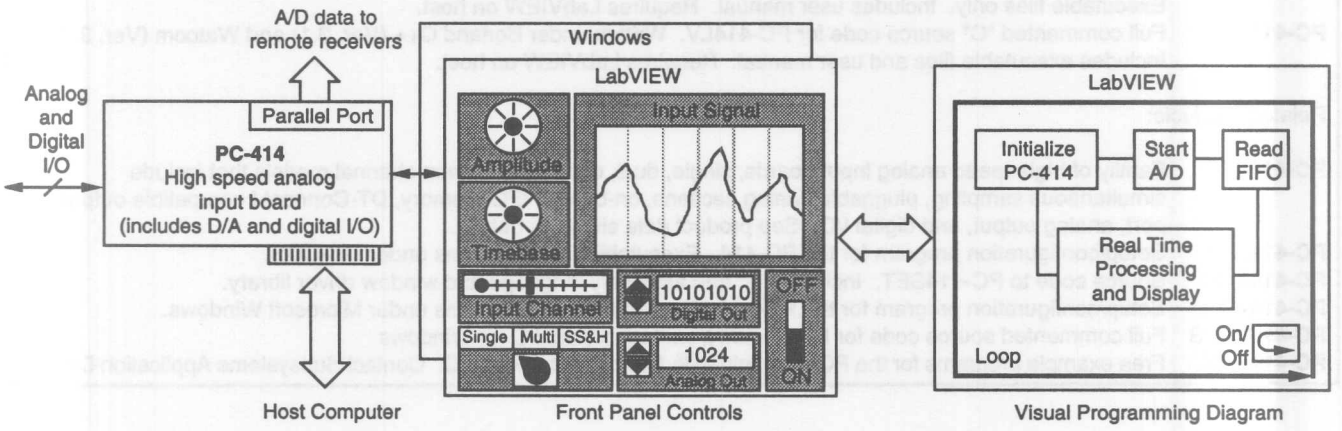


Figure 1. PC-414LV LabVIEW System Diagram

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All VI's are assembled graphically using a mouse and can be edited at any time to modify functionality or appearance. Non-stop, seamless data acquisition continues on the PC-414 while LabVIEW simultaneously maintains the GUI and handles the A/D data stream in real time. Easily customized, interactive user interfaces can be created from the vast library of front panel controls and displays offered by LabVIEW.

PC-414LV includes extensive Dynamic Linked Library (DLL) functions that perform the PC-414 low level hardware control and monitor operations transparently. The software provides VI functions that poll PC-414 status flags independent of, and simultaneous with, data acquisition and data transfer. Control is retained by the user as long as LabVIEW continues to execute correctly. The multi-window, visual programming environment facilitates building and accessing hierarchical VI programs. Multi-tasking allows context switches to other concurrent Windows applications without disrupting PC-414 operation or control.

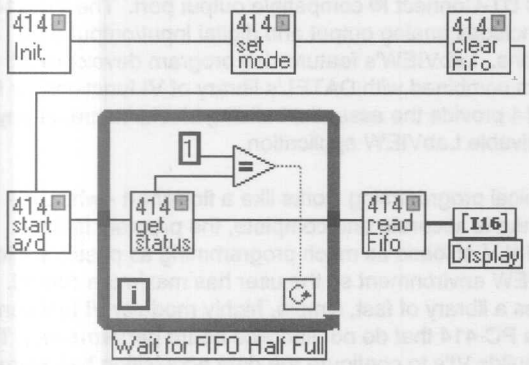


Figure 2 PC-414LV Visual Program

The PC-414LV/LabVIEW system optimizes two concurrent processes - the PC-414 acquiring data while LabVIEW further processes or stores the uploaded data stream.The entire PC-414-LabVIEW combination uses only a few VI functions that are easy to understand and incorporate into a "block diagram" program. The basic concept is to initialize the PC-414 hardware, reset the FIFO memory, start data acquisition, and upload blocks of data from the FIFO to LabVIEW memory buffers on the host - or to remote receivers over the DT-Connect I compatible output port. These data blocks can then be further processed as screen displays, indicators, graphs, sent to printers or plotters, or simply archived to disk file for later analysis. The A/D continues running and no data will be lost as long as LabVIEW uploads the A/D data faster than the data is being acquired.

Virtual Instrument Library

In summary, PC-414LV includes the following VI functions:

PC-414 Initialize	Initialize the PC-414 hardware - board model, I/O base address, etc.
Operating Mode	Specify A/D trigger rate, A/D sample rate, and analog input channel.
Clear FIFO	Reset the FIFO memory.
Start/Stop A/D	Enable and disable the A/D.
Read Status	Read hardware status flags - FIFO flags, acquisition done, oversampling.
Read FIFO	Read blocks of A/D data from the FIFO on the PC-414 and fill a LabVIEW buffer on the host.
Write DAC	Update the analog output channel.
Inport/Outport	Read/write the 8-bit digital I/O port.
PC-414 Demo	Complete data acquisition demonstration VI, includes real time signal display.
Demultiplex Buffers	Unravel a multi-channel data buffer and extract data from one channel only.

ORDERING GUIDE

All software is supplied on 3.5 inch MS-DOS diskettes.

PC-414LV	LabVIEW virtual instrument library software for DATEL's PC-414 family of high speed analog input boards. Executable files only. Includes user manual. Requires LabVIEW on host.
PC-414LVS	Full commented "C" source code for PC-414LV. Written under Borland C++ (Ver. 3.1) and Watcom (Ver. 9.01). Includes executable files and user manual. Requires LabVIEW on host.

Related products:

PC-414	Family of high speed analog input boards, single, dual, quad, and sixteen channel models that include simultaneous sampling, pluggable analog sections, on-board FIFO memory, DT-Connect I compatible output port, analog output, and digital I/O. See product data sheet for details.
PC-414SET	Setup/configuration program for the PC-414. Executable files only, runs under MS-DOS.
PC-414SRC	Source code to PC-414SET. Includes "C" and assembly language and window driver library.
PC-414WIN	Setup/configuration program for the PC-414. Executable files only, runs under Microsoft Windows.
PC-414WINS	Full commented source code for PC-414WIN, written in Visual C for Windows
PC-414BAS	Free example programs for the PC-414, written in Microsoft QuickBASIC. Contact Subsystems Application Dept.

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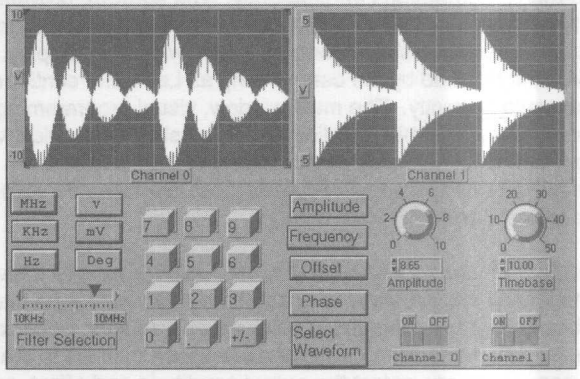
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PC-420LV

LabVIEW® Virtual Instrument Software for PC-420 Arbitrary Waveform Board

FEATURES

- **Supports DATEL's PC-420 high-speed arbitrary waveform generator board**
- **Runs under Microsoft Windows®, uses Dynamic Data Exchange (DDE)**
- **Adaptable to all National Instruments' LabVIEW applications**
- **Easy-to-use visual programming eliminates low level software**
- **Interactive, user-configured front panel controls**
- **Integrates signal creation, generation, display, and storage**
- **Dual channel update rates to 40MHz**
- **Includes digital pattern generation port**



GENERAL DESCRIPTION

National Instruments' LabVIEW transforms PC-420 high-speed arbitrary waveform generator boards into easy-to-use virtual instruments (VI's) that create, generate, store, and display any conceivable analog signals in real time. Low level software development is replaced by intuitive visual programming system that harnesses all the power of Microsoft Windows - graphic user interface (GUI), access to more host memory (16 Mbytes), multi-tasking, and inter-process communications using DDE. Applications include automatic testing, system simulation, complex control, communication signal synthesis, waveform modulation, and digital pattern testing.

The PC-420 is an ultra high-speed, very precise, arbitrary waveform generator board for IBM-PC/AT, EISAbus and compatible computers. It offers two high-performance output channels for generating complex periodic and aperiodic analog signals simultaneously. Local waveform data memory stores up to 32k samples on each channel concurrently. Data points are scanned at speeds up to 40MHz using an internal or external timebase. Separate gain and offset DAC's allow real time software control of the signal amplitude and offset.

One of seven low-pass reconstruction filters are software selectable on each channel to enhance spectral purity and minimize signal distortion. LabVIEW's feature-rich program development system combined with DATEL's library of VI functions for the PC-420 provide the essential building blocks to create any conceivable LabVIEW application.

Graphical programming works like a flowchart - when the flowchart is complete, the program is done. PC-420LV offloads as much programming as possible into the LabVIEW environment so the user has maximum control. It creates a library of fast, simple, highly modular VI functions for the PC-420 that do not sacrifice board performance. The user builds VI's to configure the hardware, generate and download the signal data files, read back and display the output waveforms without writing traditional text based programs. All VI's are assembled graphically using a mouse and can be edited at any time to modify functionality or appearance.

Non-stop, analog signal generation continues on the PC-420 while LabVIEW simultaneously maintains the GUI. Easily

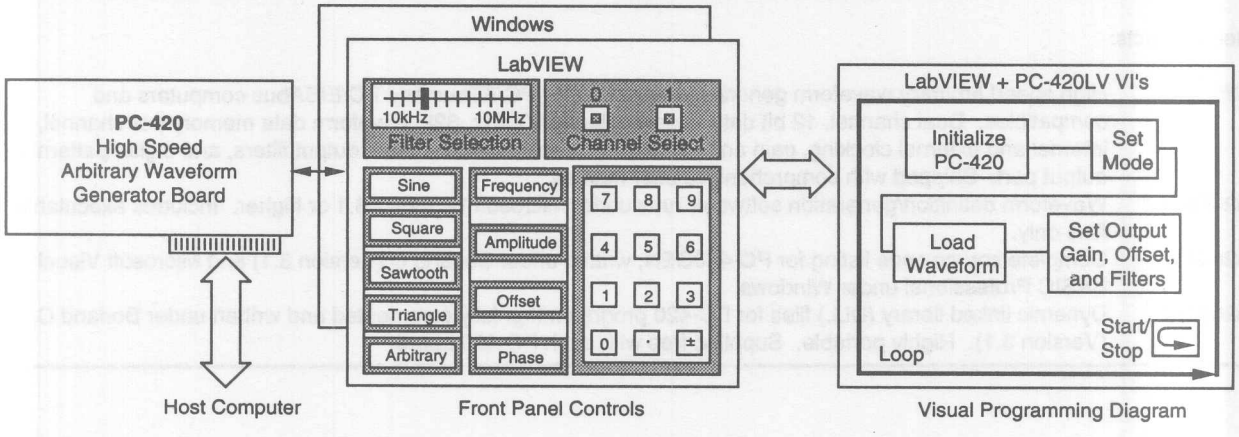


Figure 1. PC-420LV LabVIEW System Diagram

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Windows is a trademark of Microsoft
IBM-PC/AT is a trademark of IBM Corp.

customized, interactive user interfaces can be created from the vast library of front panel controls and displays offered by LabVIEW.

PC-420LV includes extensive Dynamic Linked Library (DLL) functions that perform the PC-420 low level hardware control and monitor operations transparently. The software provides VI functions that poll PC-420 status flags independent of, and simultaneous with, signal generation and waveform display. Control is retained by the user as long as LabVIEW continues to execute correctly. The multi-window, visual programming environment facilitates building and accessing hierarchical VI programs. Multi-tasking allows context switches to other concurrent Windows applications without disrupting PC-420 operation or control.

The entire PC-420LV-LabVIEW combination uses only a few VI functions that are easy to understand and incorporate into a "block diagram" program. The basic concept is to initialize the PC-420 hardware, download a waveform data file to the on-board memory, select the output amplitude and offset, and select the anti-alias low pass output filters.

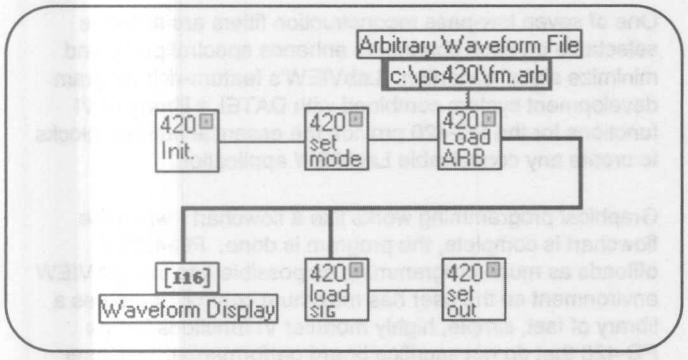


Figure 2. PC-420LV Visual Program

The PC-420 raw waveform data file can abe created in LabVIEW by an A/D board, software etc. PC-420GEN includes a powerful equation parser for creating waveform files.

Virtual Instrument Library

In summary, PC-420LV includes the following VI functions:

PC-420 Initialize	Initialize the PC-420 hardware registers and specify the I/O base address.
Operating Mode	Specify D/A clock and trigger rates, clock and trigger sources, and enable the digital pattern port.
Load Signal	Download a waveform data file to the PC-430 channel memory.
Set Output	Specify the output signal amplitude and select the optimum filter.
Read Status	Read hardware status flags - output level, phase locked loop status, etc.
Load ARB	Download arbitrary waveform file to the PC-420 memory.
Save ARB	Save an arbitrary waveform data file to disk.
Read Signal	Read the PC-420 waveform table to allow display of current signal on the host screen.
PC-420 Demo	Complete waveform data file creation and signal generation demonstration VI that includes real time signal display.

ORDERING GUIDE

All software is supplied on 3.5 inch MS-DOS diskettes.

PC-420LV	LabVIEW virtual instrument library software for DATEL's PC-420 family of high speed waveform generator boards. Executable files only. Includes user manual. Requires LabVIEW on host.
PC-420LVS	Full commented "C" source code for PC-420LV. Written under Borland C++ (Ver. 3.1) and Watcom (Ver. 9.01) compilers. Includes executable files also, shipped with a user manual. Requires LabVIEW on host.

Related products:

PC-420	High speed arbitrary waveform generator board for IBM-PC/ATbus and PC/EISAbus computers and compatibles. Dual channel, 12 bit data update rates to 40MHz, 32K waveform data memory per channel, internal and external clocking, gain and offset DAC's, software selectable output filters, and digital pattern output port. Shipped with comprehensive user manual.
PC-420GEN	Waveform definition/generation software, runs under Microsoft Windows 3.1 or higher. Includes executable files only.
PC-420SRC	Complete source code listing for PC-420GEN, written under Borland C (Version 3.1) and Microsoft Visual BASIC Professional under Windows
PC-420DRV	Dynamic linked library (DLL) files for PC-420 programming, fully commented and written under Borland C (Version 3.1). Highly portable. Supplied free with each PC-420 board.

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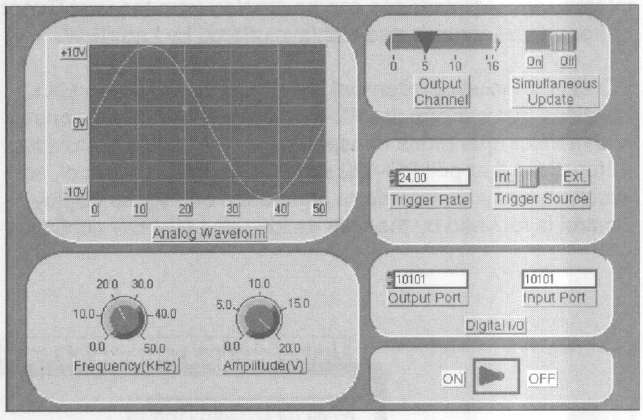
DATEL®
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PC-422LV

LabVIEW® Virtual Instrument Software for PC-422 Fast Analog Output Boards

FEATURES

- **Supports DATEL's PC-422 simultaneous analog output boards**
- **Runs under Microsoft Windows®, uses Dynamic Data Exchange (DDE)**
- **Adaptable to all National Instruments' LabVIEW applications**
- **Easy-to-use visual programming eliminates low-level software**
- **Easily customized, interactive controls and displays**
- **Choice of 8 or 16 analog outputs, 12-bit resolution**
- **Simultaneous channel update ensures phase-synchronous outputs**
- **Voltage range selectable per channel**
- **4 TTL digital inputs, 4 TTL digital outputs**



GENERAL DESCRIPTION

National Instruments' LabVIEW transforms DATEL's PC-422 high-speed simultaneous analog output boards into easy-to-use virtual instruments (VI's) that generate and display analog signals in real time. Low-level software development is replaced by an intuitive visual programming system that harnesses all the power of Microsoft Windows -- including graphic user interface (GUI), access to more host memory (16 megabytes), multi-tasking, and inter-process communications using DDE. Applications include precision system simulation, process control, audio, acoustics, and sonar.

The PC-422 is a high-speed analog output board for IBM-PC/AT, PS-30, EISA bus, and compatible computers. It offers a choice of 8 or 16 channels and it uses one 12-bit digital to analog converter (DAC) on each channel. The full scale output ranges of ±5V, ±10V, 0 to +5V, and 0 to +10V are individually selectable per channel. Each channel's data register is double buffered to allow true simultaneous update and phase-synchronous signal generation. The full scale step response of each channel is 3 microseconds, data block transfers to the input registers may occur at rates up to 1MHz. A local programmable timer provides a precision clock to sequence the output waveforms. Data sequence strobes may also be derived from an external trigger input. The PC-422 includes 8 digital input/output lines (4 in, 4 out), TTL levels.

Graphical programming works like a flowchart - when the flowchart is complete, the program is done. PC-422LV offloads as much programming as possible into the LabVIEW environment. It creates a library of fast, simple, highly modular VI functions for the PC-422 that do not sacrifice hardware performance. The user builds VI's to configure the local registers, select the trigger source and trigger rate,

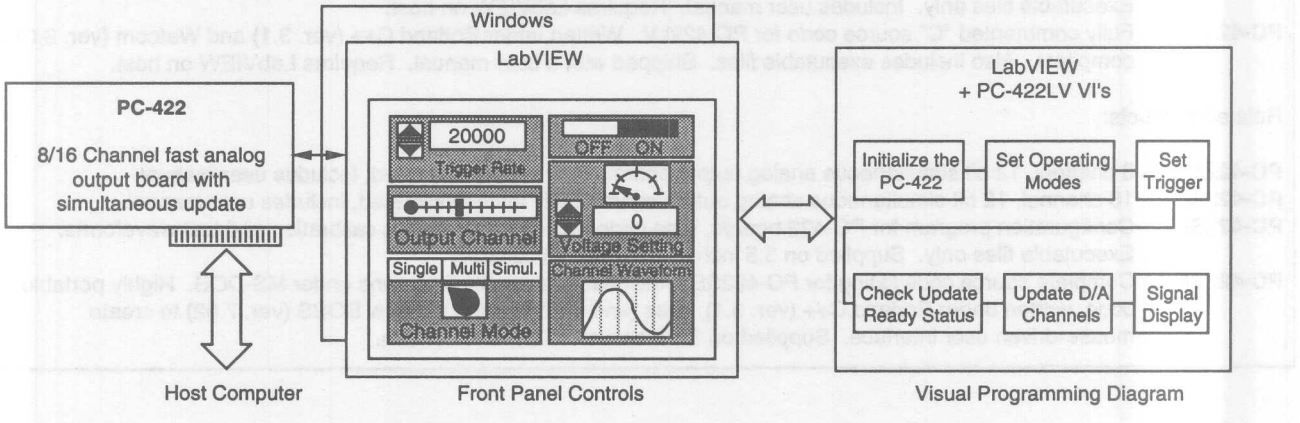


Figure 1. PC-422LV LabVIEW System Diagram

LabVIEW is a trademark of National Instruments
Windows is a trademark of Microsoft
IBM-PC/AT is a trademark of IBM Corp.

generate and display the signal data without writing traditional, text-based programs. All VI's are assembled graphically using a mouse and can be edited at any time to modify functionality or appearance. Non-stop, analog signal generation continues on the PC-422 while LabVIEW simultaneously maintains the GUI. Easily customized, interactive user interfaces can be created from the vast library of front panel controls and displays offered by LabVIEW.

PC-422LV includes extensive Dynamic Linked Library (DLL) functions that perform the PC-422 low level hardware control and monitor operations transparently. The software provides VI functions that poll PC-422 status flags independent of, and simultaneous with, waveform generation and signal display. Control is retained by the user as long as LabVIEW continues to execute correctly. The multi-window, visual programming environment facilitates building and accessing hierarchical VI programs. Multi-tasking allows context switches to other concurrent Windows applications without disrupting PC-422 operation or control.

The entire PC-422LV/LabVIEW combination uses only a few VI functions that are easy to understand and incorporate into a "block diagram" program. The basic concept is to initialize the PC-422 hardware, select the channel update mode, specify the trigger rate and source, monitor the update-ready status, and scan the data to the DAC registers.

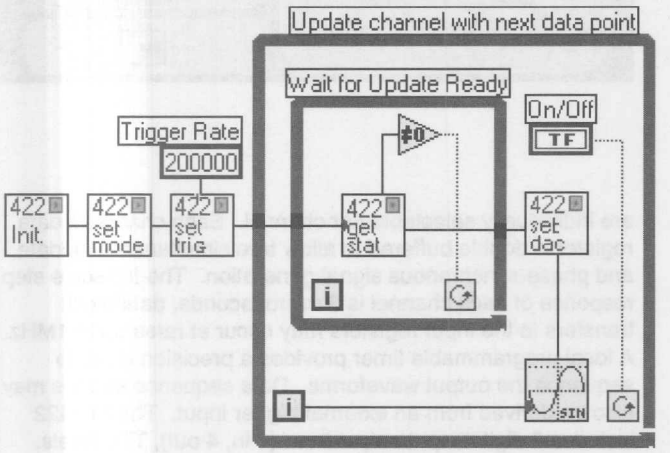


Figure 2. Typical PC-422LV Visual Program

Virtual Instrument Library

In summary, PC-422LV includes the following VI functions:

PC-422 Initialize	Initialize the PC-422 hardware registers and specify the I/O base address.
Set Mode	Select the channel update mode and trigger source.
Set Channel	Select the start channel - (0 . . . 15).
Set Trigger	Specify the internal trigger rate.
Set Simultaneous	Write simultaneous channel update control.
Set DAC	Write DAC data.
Set DACs	Write multiple DAC data words.
Read Status	Return DAC update ready, data overrun, and Command Register status.
Outport/Inport	Update/read digital I/O port.
PC-422 Demo	Analog signal generation demonstration VI, including real time signal display.

ORDERING GUIDE

All software is supplied on 3.5 inch MS-DOS diskettes.

PC-422LV	LabVIEW virtual instrument library software for DATEL's PC-422 family of high speed analog output boards. Executable files only. Includes user manual. Requires LabVIEW on host.
PC-422LVS	Fully commented "C" source code for PC-422LV. Written under Borland C++ (ver. 3.1) and Watcom (ver. 9.01) compilers. Also includes executable files. Shipped with a user manual. Requires LabVIEW on host.

Related products:

PC-422A	8 channel, 12 bit simultaneous analog output board. Fully tested/calibrated, includes user manual.
PC-422B	16 channel, 12 bit simultaneous analog output board. Fully tested/calibrated, includes user manual.
PC-422SET	Configuration program for PC-422 boards, runs under MS-DOS. Provides calibration and test waveforms. Executable files only. Supplied on 3.5 inch and 5.25 inch diskettes.
PC-422SRC	Complete source code listing for PC-422SET, includes executable files, runs under MS-DOS. Highly portable code, written under Borland C++ (ver. 3.1), uses (and includes) the Window BOSS (ver. 7.02) to create mouse-driven user interface. Supplied on 3.5 inch and 5.25 inch diskettes.

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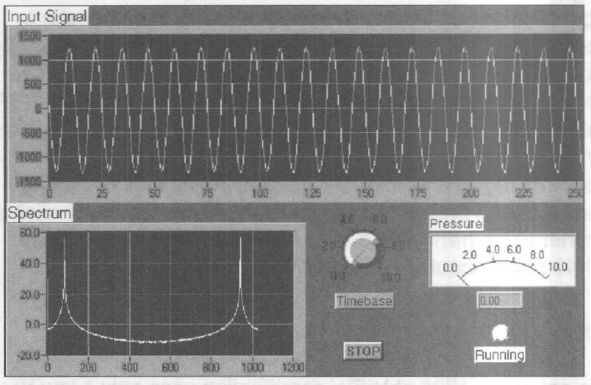
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PC-430LV

LabVIEW® Virtual Instrument Software for PC-430 A/D-DSP Boards

FEATURES

- **Supports DATEL's PC-430 A/D-DSP boards**
- **Adaptable to all LabVIEW applications**
- **Easy-to-use visual programming environment**
- **Eliminates low level software development**
- **Interactive front panel controls**
- **Integrates data acquisition, processing, display, and storage**
- **Real-time DSP, FFT's, digital filtering, etc.**
- **A/D sampling rates to 10MHz**



GENERAL DESCRIPTION

National Instruments' LabVIEW transforms the PC-430 A/D-DSP preprocessor board into an easy-to-use virtual instrument (VI) that acquires, analyzes, displays, and stores analog signals in real time. Low level software development is replaced by an intuitive visual programming system that harnesses all the power of Microsoft Windows® - graphic user interface (GUI), access to more host memory, multi-tasking, and inter-process communications.

LabVIEW's feature-rich program development system combined with DATEL's library of VI functions for the PC-430 provide the essential building blocks to create any conceivable LabVIEW application. Virtual memory usage in addition to a full 16 megabytes of host memory access means that more comprehensive application programs can be developed and larger amounts of A/D data can be collected and analyzed. Data and results can be passed using Dynamic Data Exchange (DDE) to other Windows tasks that are running simultaneously.

Graphical programming works like a flowchart - when the flowchart is complete, the program is done. PC-430LV offloads as much programming as possible into the LabVIEW environment so the user has maximum control. It creates a library of fast, simple, highly modular VI functions for the PC-430 that do not sacrifice board performance. The user builds VI's to configure the data acquisition hardware, process the data, and ultimately display and store that data without writing programs. These VI modules are assembled graphically using a mouse and can be edited at any time to modify functionality or appearance.

DATEL's Application Function Block (AFB) control programs for the DSP execute at mega-speeds internal to the PC-430 while LabVIEW simultaneously maintains the GUI and handles the A/D data stream. Easily customized, interactive user interfaces can be created from the vast library of front panel controls and displays offered by LabVIEW.

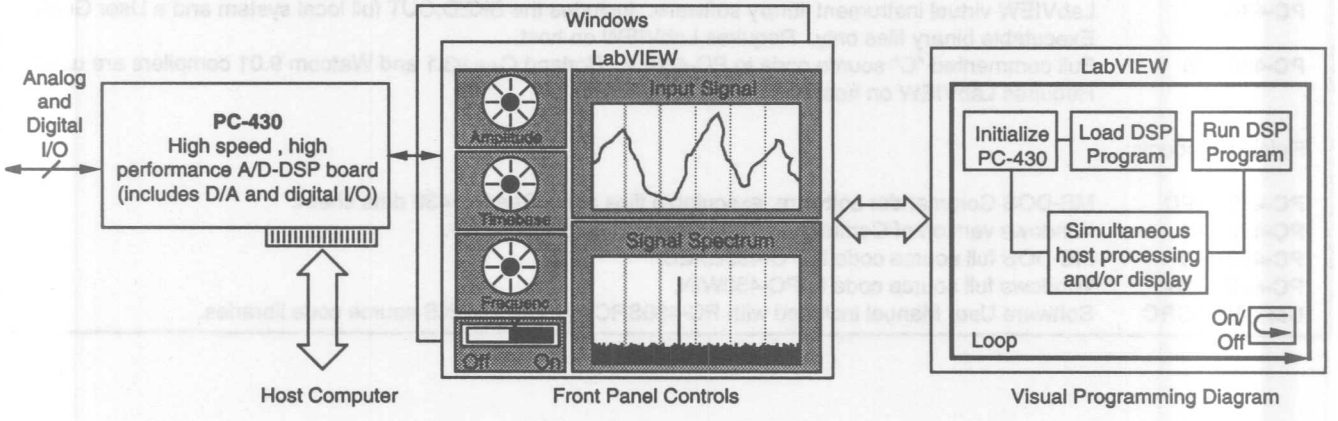


Figure 1. PC-430LV LabVIEW System Diagram

LabVIEW is a National Instruments trademark
Windows is a Microsoft trademark

PC-430LV includes extensive Dynamic Linked Library (DLL) functions that perform the PC-430 low level hardware control and monitor operations transparently. The software avoids any conditions which would lockup the system due to incorrect user programming. It provides VI functions that poll PC-430 error flags independent of, and simultaneous with, data transfer to host memory. User VI's can poll various status flags externally through LabVIEW, can count the number of pollings, and can report time-out and other error conditions due to incorrect DSP operation. Control is retained by the user as long as LabVIEW continues to execute correctly. The multi-window, visual programming environment facilitates building and accessing hierarchical VI programs. Multi-tasking allows context switches to other concurrent Windows applications without disrupting PC-430 data acquisition or control.

Application Programming

The entire PC-430/LabVIEW combination uses only a few VI functions that are easy to understand and incorporate into a "block diagram" program. The basic concept is to initialize the PC-430 hardware, download the appropriate AFB binary command file, start AFB execution, and retrieve swapped repeating uploaded data blocks from the Dual Port RAM (DPR) on the PC-430. Depending on the users AFB file these DPR blocks may be raw A/D data or the results of DSP processed arrays, e.g. FFT data, IIR/FIR filtered data, etc. The data may be presented in integer, long, or floating point format. Data blocks are loaded into LabVIEW buffers where they can be further processed as screen displays, indicators, graphs, sent to printers or plotters, or simply archived to disk file for later analysis.

The system optimizes two concurrent processes - the PC-430 acquiring and processing A/D data while LabVIEW further processes or stores the uploaded data stream. PC-430LV functions use a swapped, double buffer arrangement where the DSP is processing one buffer while LabVIEW is uploading the other buffer in the pair. The buffers can be almost any type and size. PC-430 throughput will depend on the A/D sampling rate and degree of internal DSP processing specified in the users AFB file. The A/D continues running and no data will be lost as long as LabVIEW uploads the DPR buffers fast enough. The PC-430/LabVIEW combination offers true coprocessing.

Virtual Instrument Library

PC-430LV includes the following VI functions:

PC-430 Initialize	Initialize the PC-430 hardware - configure hardware, test DSP memory, download DSP executive, verify proper DSP boot sequence, etc.
Load AFB File	Download an AFB binary file to the PC-430 .
Run AFB File	Start AFB execution on the DSP - data acquisition, DSP processing.
Read Status	Monitor PC-430 status flags - buffer ready, overflow, errors.
Read DPR	Transfer a DPR data buffer from the PC-430 to a specified LabVIEW buffer at maximum speed. 16 bit, 32 bit, and single precision floating point transfer options are provided.
Stop AFB	Halt internal DSP program execution - AFB done or error has occurred.
Read DPR	Read the contents of a DPR memory location.
Write DPR	Write data to a DPR memory location.
Demultiplex Buffers	Unravel a multi-channel data buffer and extract data from one channel only - similar to decimation except only one channel is extracted.

ORDERING GUIDE

All software is supplied on 3.5-inch MS-DOS diskettes.

PC-430LV	LabVIEW virtual instrument library software. Includes the SKED.OUT full local system and a User Guide. Executable binary files only. Requires LabVIEW on host.
PC-430LVS	Full commented "C" source code to PC-430LV. Borland C++ v3.1 and Watcom 9.01 compilers are used. Requires LabVIEW on host.

Related products:

PC-430EXEC	MS-DOS Commander software, executable files only. See PC-430 data sheet.
PC-430WIN	Windows version of Commander software, executable files only.
PC-430SRC	MS-DOS full source code to PC-430EXEC.
PC-430WINS	Windows full source code to PC-430WIN.
UM-CMDRSRC	Software User Manual included with PC-430SRC or PC-430WINS source code libraries.

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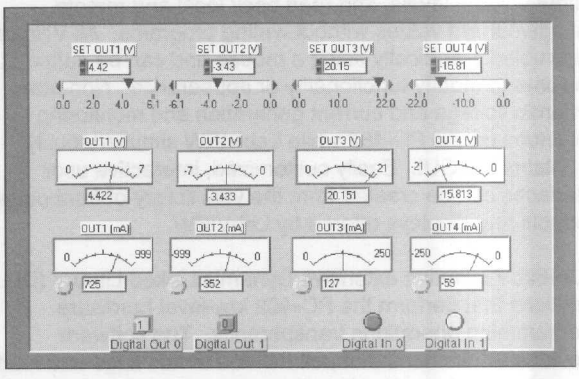
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PC-462LV

LabVIEW® Virtual Instrument Software for PC-462 Programmable Power Supply

FEATURES

- **Supports DATEL's PC-462 precision programmable power supply board for PC/AT bus computers**
- **Runs under Microsoft Windows®, uses Dynamic Data Exchange (DDE)**
- **Adaptable to all National Instruments LabVIEW applications**
- **Easy-to-use visual programming eliminates low-level software**
- **Integrates current and voltage generation, monitoring, and display**
- **4 independently programmable voltage outputs**
- **Includes current limiting and remote sensing**
- **Dedicated and general purpose analog input and digital I/O**
- **All channels fully isolated from the host computer**



GENERAL DESCRIPTION

National Insutrments' LabVIEW transforms DATEL's PC-462 high-precision programmable power supply boards into easy-to-use virtual instruments (VI's) that generate and monitor current and voltage levels in real time. Low-level software development is replaced by an intuitive visual programming system that harnesses all the power of Microsoft Windows including graphic user interface (GUI), access to more host memory (16 megabytes), multi-tasking, and inter-process communications using DDE. Typical applications include laboratory power sourcing, automated dynamic testing, motor control, calibration, simulation, relay switching, and thermocouple characterization.

The PC-462 is a high-precision, low-cost, programmable power supply board for IBM-PC/AT, PS-30, EISA bus, and compatible computers. Four output channels can be individually selected by software for ranges up to ±6.1425V at 1 Amp and up to ±20.475V at 250 milliamps. Each channel includes output current limiting that protects it from overload and short circuit conditions while remote voltage sensing allows regulation with respect to the load. Local voltage and current levels can be monitored in real time by host software.

Four general purpose analog input channels as well as four digital I/O lines are provided for monitor and control of external devices. Two MOSFET digital output lines can switch loads up to 300V at 100 milliamps, making them ideal for switching relays and triac circuits. All input and output channels provide 250V rms isolation from the PC bus. LabVIEW's feature-rich program development system combined with DATEL's library of VI functions in PC-462LV provide the essential building blocks to create any conceivable LabVIEW application using the PC-462 board.

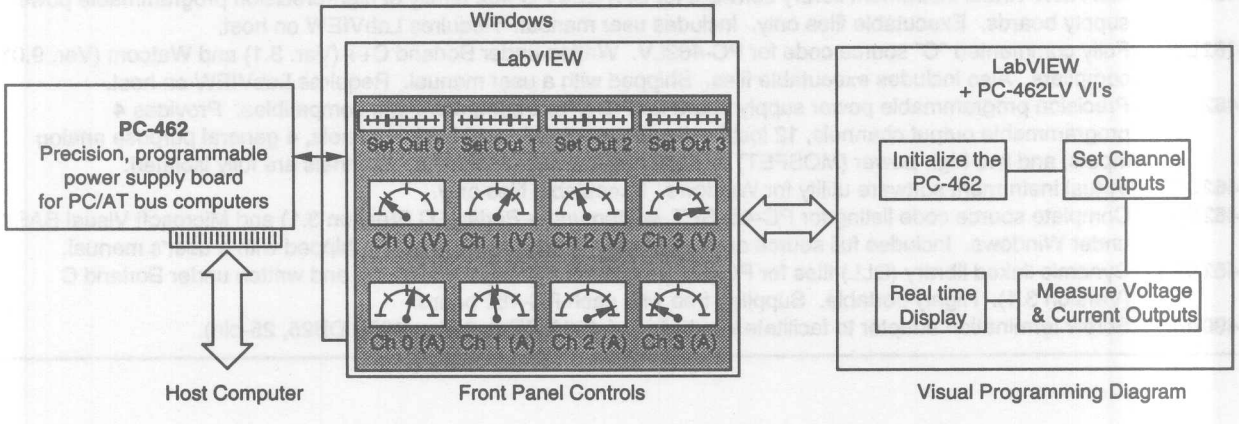


Figure 1. PC-422LV LabVIEW System Diagram

LabVIEW is a trademark of National Instruments
Windows is a trademark of Microsoft
IBM-PC/AT is a trademark of IBM Corp.

Graphical programming works like a flowchart - when the flowchart is complete, the program is done. PC-462LV offloads as much programming as possible into the LabVIEW environment so the user has maximum control. It creates a library of fast, simple, highly modular VI functions for the PC-462 that do not sacrifice board performance. The user builds VI's to configure the hardware, generate different output voltage levels, and read back local and remote voltage/current values without writing programs. All VI's are assembled graphically using a mouse and can be edited at any time to modify functionality or appearance. Non-stop, dynamic voltage and current generation and monitoring continues on the PC-462 while LabVIEW simultaneously maintains the GUI. Easily customized, interactive user interfaces can be created from the vast library of front panel controls and displays offered by LabVIEW.

PC-462LV includes extensive Dynamic Linked Library (DLL) functions that perform the PC-462 low-level hardware programming operations transparently. The software provides VI functions that poll PC-462 status flags and read current and voltage levels independent of, and simultaneous with, power waveform generation and display. Control is retained by the user as long as LabVIEW continues to execute correctly. The multi-window, visual programming environment facilitates building and accessing hierarchical VI programs. Multi-tasking allows context switches to other concurrent Windows applications without interrupting PC-462 operation. DDE facilitates data exchange with other software programs, e.g. spreadsheets for data logging.

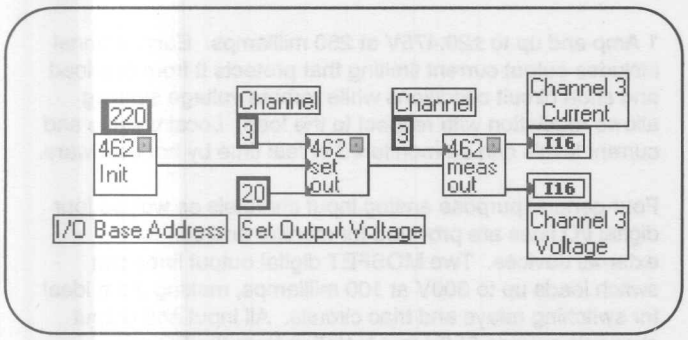


Figure 2 Typical PC-462LV Visual Program

The entire PC-462LV-LabVIEW combination uses only a few VI functions that are easy to understand and incorporate into a "block diagram" program. The basic concept is to initialize the PC-462 hardware and set up the voltage on each of the four output channels. VI's are also supplied to monitor local and external voltage and current levels in real time. Figure 2 illustrates the simplicity of the VI programming system

Virtual Instrument Library

In summary, PC-462LV includes the following VI functions:

PC-462 Initialize	Initialize the PC-462 hardware.
Set Trigger Source	Select internal or external triggering for the A/D section, i.e. current/ voltage read back.
Update Outputs	Set the output voltage levels.
Measure Outputs	Monitor the local current and voltage levels on each channel.
Read A/D Channels	Read the analog levels on the general purpose A/D input lines.
Digital Outport	Update the digital output lines.
Digital Inport	Read the digital input lines.
Set A/D Channel	Specify different analog input channels.
Start A/D	Start the A/D converter.
Read Status	Return the A/D conversion status.
Read A/D Data	Read the A/D data when a conversion is complete.
PC-462 Demo	Complete voltage setup and real-time monitor demonstration VI.

ORDERING GUIDE

All software is supplied on 3.5 inch MS-DOS diskettes.

PC-462LV	LabVIEW virtual instrument library software for DATEL's PC-462 family of high-precision programmable power supply boards. Executable files only. Includes user manual. Requires LabVIEW on host.
PC-462LVS	Fully commented "C" source code for PC-462LV. Written under Borland C++ (Ver. 3.1) and Watcom (Ver. 9.01) compilers. Also includes executable files. Shipped with a user manual. Requires LabVIEW on host.
PC-462	Precision programmable power supply board for PC/ATbus computers and compatibles. Provides 4 programmable output channels, 12 local voltage/current A/D read-back channels, 4 general purpose analog inputs, and two high-power (MOSFET) digital input and output lines. All channels are fully isolated.
PC-462SET	Virtual instrument software utility for Windows. Executable files only.
PC-462SRC	Complete source code listing for PC-462SET, written under Borland C (Version 3.1) and Microsoft Visual BASIC under Windows. Includes full source and executable files. The software is shipped with a user's manual.
PC-462DRV	Dynamic linked library (DLL) files for PC-462 programming, fully commented and written under Borland C (Version 3.1). Highly portable. Supplied free with each PC-462 board.
PC-490A/B	Screw termination adapter to facilitate input/wiring (-490A DB-9, 9 pin, -490B DB25, 25-pin).

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PC-430HYPER

Integrated Control, Storage, and Display Software for DATEL's PC-430 Boards

FEATURES

- **Real-time data collection, processing, display, and storage**
- **Integrated Digital Signal Processing environment**
- **A/D sample rates up to 4MHz**
- **Dual-channel digital oscilloscope and spectrum analyzer**
- **DSP accelerated FFT and inverse FFT processing**
- **Digital filter design, simulation, code generation**
- **"Snap-in" real-time digital filtering**
- **High-speed data streaming to disk**
- **Comprehensive analog signal data file processing**
- **2-D and 3-D spectrographic analysis**



GENERAL DESCRIPTION

PC-430HYPER complements DATEL's full offering of software development tools for the PC-430 family of high-speed, A/D-DSP co-processor boards. It is a complete, integrated DSP environment that achieves simultaneous hardware control, data analysis, graphical display and report generation. This powerful utility operates on all PC/AT/286/386/486, PS-30, EISA bus and compatible host computers, running MS-DOS 3.0 (or higher). PC-430HYPER accomodates all features of the PC-430 family but shields users from all the low level programming details.

An intuitive menu system guides the user from initial system configuration through A/D data collection to data analysis, display, and storage. Configuration files covering all aspects of host setup, memory configuration, and DSP selection can be stored for automatic re-configuration each time PC-430HYPER is invoked. The system supports over 100 different graphics hardware configurations including CGA, EGA, VGA, Super VGA, and Hercules, as well as high publication-quality output to over 200 printer models including HP's LaserJet and PaintJet color printers.

After specifying A/D parameters such as sampling rate (4MHz max.) and sample counts, DSP data processing, data display and data file generation may be performed on a live or historical basis. Single or dual channel digital oscilloscope and spectrum analyzer displays are available in real time. They include independently controlled dual trace displays which take their input from the PC-430 A/D channels or from waveform disk files. The trigger level and channel, timebase, offset scaling, sampling rate and input voltage ranges are all selectable. A real-time 3-D Map Analyzer ("running waterfall") is also included.

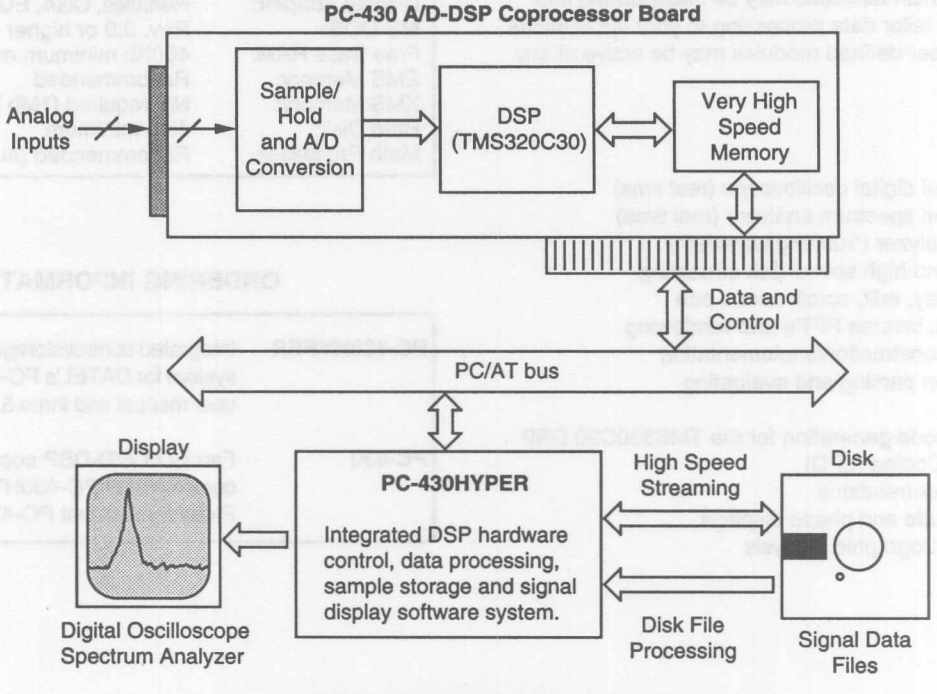


Figure 1. PC-430HYPER Application Diagram

Classical lowpass, highpass, bandpass, bandstop and arbitrary frequency response FIR and IIR filters may be designed graphically or using complex difference equations. They can be "snapped-in" to operate on real-time data from the analog inputs on the PC-430 board - accelerated by the local DSP.

The user has full control over all filter parameters such as cutoff frequency, passband ripple, stopband attenuation, stopband rolloff, etc. A powerful code generator for FIR and IIR filters produces optimized, ready-to-assemble source code text files for the Texas Instruments TMS320C30 DSP on the PC-430 board, with a choice of native assembly language or 'C' code output. The filter's quantized frequency and impulse response may be simulated and displayed.

Signal data acquired in real time acquisition can be streamed continuously to a hard disk at rates up to 150kHz, or to RAM disks at rates in excess of 200kHz. PC-430 data files may be converted between binary, ASCII, hexadecimal, and floating point representations compatible with common spreadsheet programs, text editors, modem transmissions, etc. Archived data files can be analyzed, huge data files may be displayed, and sections of time waveforms may be selected and edited. Powerful zoom facilities enlarge areas containing critical information. To complement the true multichannel capabilities of the PC-430 hardware, PC-430HYPER supports multi-channel data acquisition and de-multiplexes each channel's data into separate files. Intra-channel displays include simultaneous combinations of magnitude, phase, power spectra, and time. The trigger channel and levels are selectable as are positive and negative trigger delays.

The learning process is minimized by a powerful, context-related HELP utility that can be activated at the press of a key. A mouse can be used for making selections, waveform editing, filter construction, etc. User-defined time and frequency domain functions may be incorporated into PC-430HYPER to tailor data processing to your applications and six external user-defined modules may be active at any one time.

FUNCTIONS

Single/dual channel digital oscilloscope (real time)
Single/dual channel spectrum analyzer (real time)
Real-time Map Analyzer ("running waterfall")
Data acquisition and high speed disk streaming
Disk file time display, edit, scroll, zoom, pan
Accelerated FFT's, inverse FFT's and windowing
FIR and IIR filter construction/implementation
Difference equation parsing and evaluating
Recursive filtering
FIR and IIR filter code generation for the TMS320C30 DSP
Linear Predictive Coding (LPC)
Convolutions and correlations
Pole zero, magnitude and phase displays
2-D and 3-D Spectrographic analysis

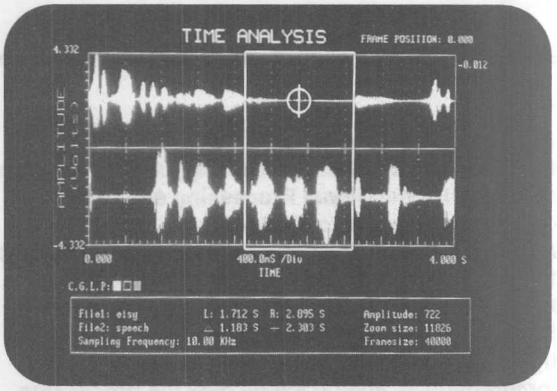


Figure 2. Time Analysis

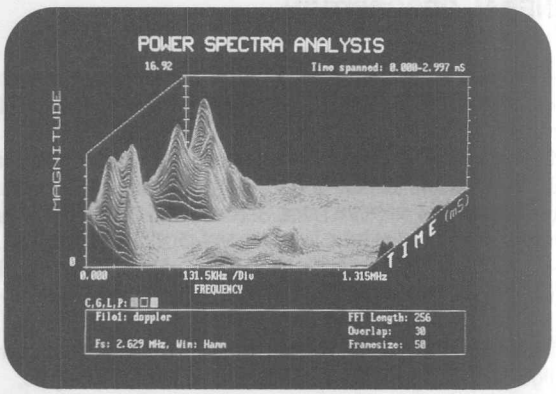


Figure 3. Power Spectra

SYSTEM REQUIREMENTS	
Display Adapter:	Hercules, CGA, EGA, VGA,SVGA etc.
MS-DOS:	Rev. 3.0 or higher
Free Base RAM:	400Kb minimum recommended
EMS Memory:	Recommended
XMS Memory:	Not required (1Mb XMS must be free)
Hard Disk:	4Mb minimum
Math Processor:	Recommended (autodetect)

ORDERING INFORMATION

PC-430HYPER	Integrated control/storage/display software system for DATEL's PC-430 family. Includes user manual and three 5.25" HD disks.
PC-430	Family of A/D-DSP coprocessor boards controlled by PC-430HYPER. Please see latest PC-430 data sheet.

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PC-"SET" Series

- Low-cost, easy-to-use setup, configuration, data save/load software for PC-411, 412, 414, 462, 422, 415, 420.
- Save data to disk or memory at rates exceeding 1MHz. Full source code available ("SRC" series). MS-DOS or WINDOWS.
- Windowed "no-programming" menu interface. File output to PC-DADiSP or spreadsheets.
- Batchable autorun mode.

PC-DADiSP

- High-quality, file input A/D data graphics display and analysis worksheet software.
- Use with any A/D signal file. Extensive math library, over 300 functions, FFT's, filters, 3D plotting, etc.
- Powerful macro math language, multi-Window displays, publication-quality graphics output.

PC-430HYPER

- High-performance real-time data acquisition, graphics display, data file save/playback and DSP library for DATEL's PC-430.
- Multi-channel digital oscilloscope, spectrum analyzer, FFT display, digital filtering, autocorrelation, code generation, and many more!

PC-430LV, PC-412LV, PC-414LV, PC-420LV, PC-422LV, and PC-462LV

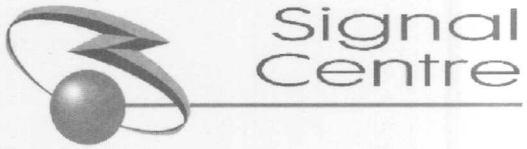
- LabVIEW® Virtual Instrument software library for DATEL's boards.
- Includes fast, low-level, graphic, block diagram programming functions.
- Adaptable to all LabVIEW® applications.
- Ideal for high-performance data acquisition, DSP, FFT's, digital filtering, etc.
- Implements non-stop "streaming" of A/D data to disk, graphic screen or control loops.

LabVIEW® is a trademark of National Instruments

High-Performance Software is also available from these DATEL Partners. Contact DATEL for information.

PROSIG

- Prosig - The clearest picture in spreadsheet signal processing.
- Supports DATEL PC-411/412 and PC-414 A/D-FIFO boards.
- Ideal "what if?" processor. Store analysis steps directly in a spreadsheet.
- Easy learning and fast results ... intuitive interface ... rich, windowed test environment. Get results minutes after installation.
- WYSIWYG graphics ... add your text then plot in background while collecting the next A/D data set.
- Applications: vibration studies, acoustics and speech analysis, medical/biological research, structural dynamics/analysis, etc.



- Signal Centre - Easy-to-use, "no programming," block diagram A/D-D/A software
- Watch your data, through multiple viewports, as it is collected.
- Link signals, events and triggers together with structure dialogue boxes.
- High-quality screen display and presentation plotting.
- Powerful, logical, statistics and math libraries.
- Turn-key "load and go." Log data to disk, simulate an instrument, etc.

Contact **DATEL** for:

- High-Performance Data Acquisition and Control Boards
- High-Speed/Resolution Data Conversion Components
- Modular DC/DC Power Converters
- Digital Panel Voltmeters and Instruments

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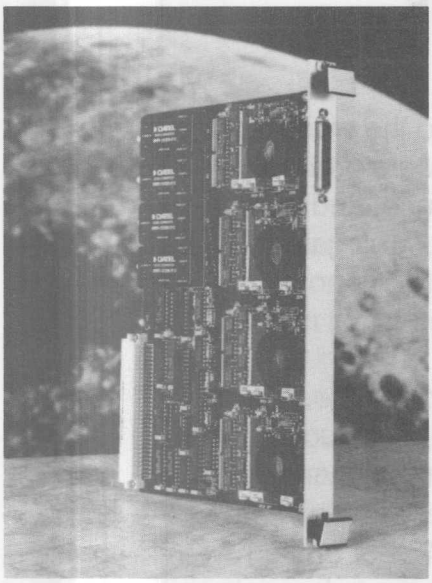
Analog Boards for VME Bus

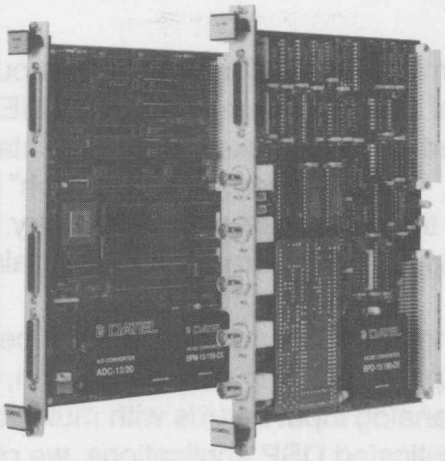
VME continues to be the premier, high-performance bus around the world, and DATEL continues to be one of its strongest supporters. VME users prefer its strong standardization, rugged pin-and-socket backplane interface, and wide variety of host CPU systems. Once considered a "research" bus relegated to government laboratories and the military/aerospace industry, VME is now the preferred bus for advanced applications in many commercial/industrial markets.

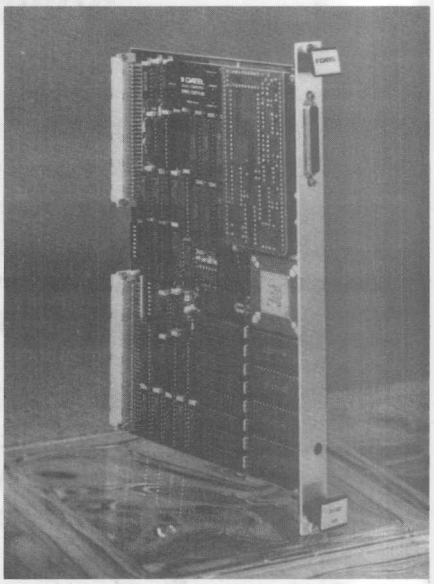
DATEL designs, develops, and manufactures quality, high-performance, analog boards for all types of VME applications. In data acquisition, our products include high-speed, high-resolution, analog input boards with multiple input channels and on-board memory. For sophisticated DSP applications, we offer analog input boards with on-board DSP coprocessors and expansion SRAM. For analog outputs, we offer signal-generator boards with as many as 16 output channels as well as fully isolated, quad-output, powersupply boards.

We give patient, experienced, applications assistance and willingly "customize" standard products for OEM applications. Consider DATEL products for your next VME application.

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Fully Isolated, Precision 4-Channel, Programmable Power Supply Board

DVME-621

- 4 independently programmable, voltage/current outputs:
  0 to +11V, ±11V @ 100mA
  0 to +20/50/160mA, ±160mA
- Highly accurate, 12-bit D/A for each channel
- Digital inputs to D/A's opto isolated from data bus
- Each D/A powered by fully isolated DC/DC converter
- 500Vrms channel-to-channel and channel-to-bus isolation
- Output overvoltage and short-circuit protection
- Remote sensing for each output
- Ideal for process control and industrial automation

See page 2-29

2-Channel, 14-Bit, 1-2MHz Simultaneous Sampling Analog Input Board

"G" Models of DVME-614/630

- 2 parallel analog input channels with simultaneous sampling
- 2 independent, 1MHz, 14-bit A/D converters (2MHz optional)
- 500kHz input bandwidths
- –80dB total harmonic distortion
- Ideal for DSP FFT applications
- On-board A/D FIFO memory up to 16k samples for non-stop data "streaming" to disk
- Throughput to FIFO:
  1MHz (single channel)
  2MHz (simultaneous channels)
- On-board TI 320C30 (32/40MHz) DSP (model DVME-630G)

See pages 2-21, 49

Capture and Analyze Analog Signals with Advanced A/D-DSP Coprocessor

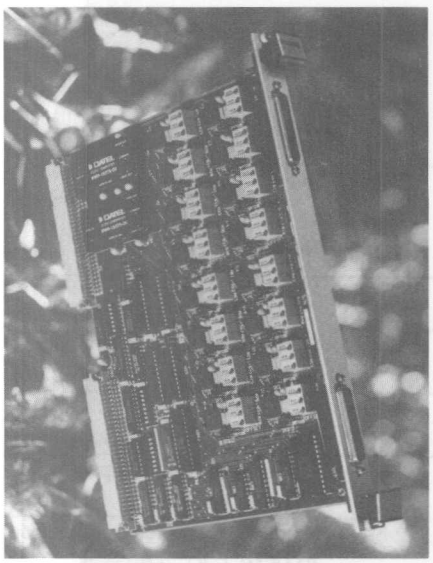
DVME-630 Family

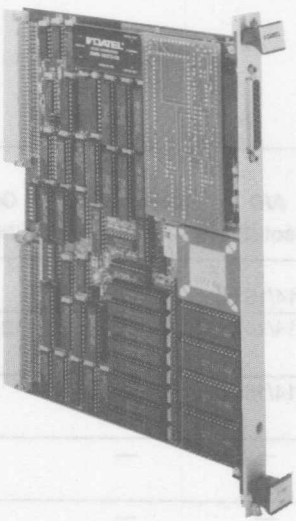
- Up to 16SE/8D analog input channels
- Up to 10MHz A/D sampling rates
- Choice of 12 or 14-bit A/D resolutions
- 2/4/8-channel simultaneous sampling
- Local FIFO up to 4k A/D samples
- On-board TI 320C30 (32/40MHz) digital signal processor
- Two, 12-bit D/A channels (optional)
- Digital I/O (16 in, 16 out) (optional)
- Up to 4.5Mb dual-port RAM
- Vectored interrupt to VME host
- On-board DSP library - FFT's windowing, filters, floating point, etc.
- Fast, simple, powerful Command Executive - no local programming

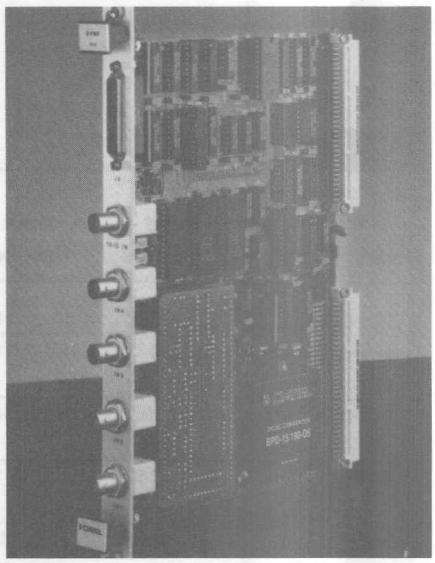
See page 2-49

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New Products







Generate 16 Fast Simultaneous Analog Outputs

DVME-622

- 8 or 16 analog outputs from independent, 12-bit D/A's
- Individually selectable output ranges per channel:
  0 to +5V, 0 to +10V
  ±2.5V, ±5V, ±10V
- Double buffered digital input registers
- High-speed simultaneous block loading
- Simultaneous update for phase tracking and skew elimination
- On-board update clock or external event synchronization
- 3µsec settling, 330kHz update rate
- ±0.025% output linearity
- Trigger timer interrupt
- Discrete digital I/O (4 in, 3 out)
- Ideal for coherent waveform generation

See page 2-33

8-Channel, 12-Bit, 250kHz Simultaneous Sampling Analog Input Board

"J" Models of DVME-614/630

- 8 parallel analog input channels with concurrent sampling
- 8 independent, 12-bit, 250kHz A/D converters
- Eliminate phase skew on 8 parallel channels
- 100kHz input bandwidths
- –77dB total harmonic distortion
- Ideal for DSP/FFT applications
- On-board A/D FIFO memory up to 16k samples for non-stop data "streaming" to disk
- Throughput to FIFO:
  250kHz (single channel)
  2MHz (simultaneous channels)
- On-board TI 320C30 (32/40MHz) DSP (model DVME-630J)

See page 2-21, 49

Collect Millions of High-Speed, Analog Samples to Disk or Memory

DVME-614 Family

- Up to 16 analog input channels
- Up to 10MHz A/D sampling rates
- Choice of 12 or 14-bit A/D resolutions
- 2/4/8-channel simultaneous sampling eliminates phase skew
- Programmable-threshold analog input trigger
- On-board FIFO up to 16k A/D samples for non-stop, gapless, data "streaming" to disk
- 4MHz parallel port avoids bus delays
- Direct streaming to host memory to 64Mb or greater
- Very low harmonic distortion - ideal for DSP/FFT applications
- Excellent array-processor "front end"

See page 2-21

VME bus Selection Tables

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Data Acquisition

Model	Input Channels	Input Ranges	A/D Resolution	A/D Conversion Rate	Output Channels	Page Number	Notes
DVME-611 Series	32SE/16D	40mV to 10V①	12/14/16 bits	To 400kHz	—	2-7	Expandable to 256SE/128D chans.
DVME-612 Series	32SE/16D	40mV to 10V①	12/14/16 bits	To 400kHz	2, 12-bit D/A's	2-7	80dB CMRR, 2TTL digital outputs on-board interrupt vector registers
DVME-613 Series	16SE/8D isolated	50mV to 10V②	12/14/16 bits	To 40kHz	—	2-15	500V isolation, digital I/O (8 in, 8 out), vectored interrupt, A/D clock
DVME-641	32SE/16D	50mV to 10V	—	—	—	2-57	Slave A/D channel expander for 611/612, cascadable
DVME-643T	8 thermo-couples isolated	25mV to 100mV	—	—	—	2-59	Slave A/D channel expander for 611/612, CJC, 750V isolation
DVME-643H	8D isolated	±5V	—	—	—	2-59	Slave A/D channel expander for 611/612, 750V isolation
DVME-645	16SE/8D	±10V	—	—	—	2-61	Slave A/D channel expander for 611/612, 16 simultaneous S/H

①Software-selectable gain in 8 ranges from 1 to 128. ②Gain of 1, 10, or 100 is jumper-selectable.

High-Speed A/D Plus Memory

See page 2-21

Model	Input Channels	Input Ranges	A/D Resolution	A/D Conversion Rate	Output Channels	Data Memory	Notes
DVME-614A	4SE simul.	0 to +1V/10V①, ±1V/10V	12 bits	To 1.5MHz/chan.	1, 12-bit D/A	To 16ks FIFO	All models of the DVME-614 have a programmable trigger/ counter and a 10MHz parallel port. All have an on-board, 12-bit D/A (200kHz update rate) and a programmable-threshold analog trigger.
DVME-614B	4SE	0 to +10V, ±5V, ±10V	14 bits	To 500kHz	1, 12-bit D/A	To 16ks FIFO	
DVME-614C	4SE	0 to +10V ±5V, ±10V	12 bits	To 1.6MHz	1, 12-bit D/A	To 16ks FIFO	
DVME-614D	1D	±5V	12 bits	To 5MHz	1, 12-bit D/A	To 16ks FIFO	
DMVE-614E	16SE/8D	50mV to 10V②	12 bits	To 2MHz	1, 12-bit D/A	To 16ks FIFO	
DVME-614F	2SE simul.	0 to +10V, ±5V	12 bits	To 2MHz/chan.	1, 12-bit D/A	To 16ks FIFO	
DVME-614G	2SE simul.	0 to +10V, ±5V	14 bits	To 2MHz/chan.	1, 12-bit D/A	To 16ks FIFO	
DVME-614H	1D	±5V	12 bits	To 10MHz	1, 12-bit D/A	To 16ks FIFO	
DVME-614J	8SE simul.	0 to +2.5, ±5V, ±10V	12 bits	To 250kHz/chan.	1, 12-bit D/A	To 16ks FIFO	

①Gains of 1 or 10 are user-selectable on 2 channels. ②Gain of 1 to 100 is resistor-programmable.

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VME bus Selection Tables

Fast A/D-DSP Coprocessor

See page 2-49

Model	Input Channels	Input Ranges	A/D Resolution	A/D Conversion Rate	Output Channels	Data Memory	Notes
DVME-630A	4SE simul.	0 to +1V/10V, ±1V/10V①	12 bits	To 1.5MHz/chan.	—	To 4ks FIFO	All models of the DVME-630 incorporate a 32MHz (40MHz opt.) TI320C30 DSP CPU operating on a local 32-bit data bus. All have installed 1/2Mb dual-port SRAM expandable to 4.5Mb with MEM-30. All have an on-board, programmable timer/counter and offer multiple triggering schemes.
DVME-630B	4SE	0 to +10V, ±5V, ±10V	14 bits	To 500kHz	—	To 4ks FIFO	
DVME-630C	4SE	0 to +10V, ±5V ±10V	12 bits	To 1.6MHz	—	To 4ks FIFO	
DVME-630D	1D	±5V	12 bits	To 5MHz	—	To 4ks FIFO	
DVME-630E	16SE/8D	50mV to 10V②	12 bits	To 2MHz	—	To 4ks FIFO	
DVME-630F	2SE simul.	0 to +10V, ±5V	12 bits	To 2MHz/chan.	—	To 4ks FIFO	
DVME-630G	2SE simul.	0 to +10V, ±5V	14 bits	To 2MHz/chan.	—	To 4ks FIFO	
DVME-630H	1D	±5V	12 bits	To 10MHz	—	To 4ks FIFO	
DVME-630J	8SE simul.	0 to +2.5V, ±5V, ±10V	12 bits	To 250kHz/chan.	—	To 4ks FIFO	
PC-430DAC	—	0 to +5V/10V, ±5V/10V③	—	100kHz④	2, 12-bit D/A's	—	DVME-630 serial-port daughter modules, dual DAC or digital I/O. *See page 1-55*
PC-430DIG	16 TTL	Digital I/O	—	To 500kHz	16 TTL	—	
MEM-30/30B	1Mb or 4Mb SRAM memory expander module for DVME-630. *See page 2-73*						

①Gains of 1 or 10 are user-selectable on 2 channels. ②Gain of 1 to 100 is resistor-programmable. ③Output voltage ranges. ④D/A update rate.

Analog Output and Special Functions

Model	Output Channels	Output Ranges	D/A Resolution	D/A Conversion Rate	Notes
DVME-628V	8 D/A	0 to +5V, +10V, ±2.5V, ±5V, ±10V	12 bits	167kHz	A16:D16 slave. *See page 2-45*
DVME-628C	8 D/A	Same as above plus 4-20mA	12 bits	167kHz	A16:D16 slave, passive current loops 15-36V external excitation. *See page 2-45*
DVME-626V	6 D/A	0 to +10V, ±5V, ±10V	16 bits	67kHz	A16:D16 slave, ±0.005% linearity. *See page 2-41*
DVME-621	4 D/A isolated	0 to +11V, ±11V, 0 to +160mA, ±160mA	12 bits	91kHz	A24:D16 slave, active loop mode, 500V rms isolation. *See page 2-29*
DVME-622	8 or 16 D/A	0 to +5V, +10V, ±2.5V ±5V, ±10V	12 bits	330kHz	A24:D16 slave, simultaneous update, trigger/timer interrupt. *See page 2-33*
DVME-660	48-line digital I/O	TTL logic	—	To 4 Mword/sec	A16:D16 slave, 24-stage timer/interrupt, programmable direction by byte. *See page 2-63*
DVME-691	Rack-mount signal conditioning screw terminator with flat cables for all DATEL VME boards. *See page 2-67*				

VME bus Selection Tables

DATEL® INNOVATION and EXCELLENCE

Software

Model	Host Board	Format	Description
DVME-622SRC	DVME-622	MS-DOS ASCII source disk	Highly portable "C" and 680X0 assembly language comprehensive data playback system for UNIX. Rich function library.
	DVME-614, -613	MS-DOS ASCII source disk	Highly portable "C" and 680X0 assembly language program examples. Included with board or FREE on request. OS-9/UNIX device drivers.
DVME-630EXEC	DVME-630	MS-DOS ASCII source disk	High-speed data recorder for UNIX hosts. Highly portable "C" and 680X0 assembly language with rich DSP library. Host side is source format. DVME-630 side is downloadable binary.
DVME-630SRC	DVME-630	MS-DOS ASCII source disk	Same as above except full source code.

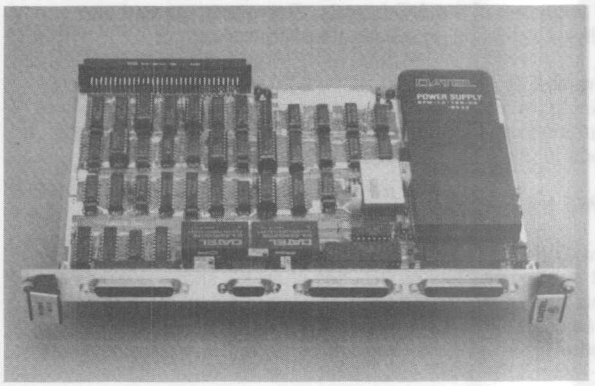
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DATEL®
INNOVATION and EXCELLENCE

DVME-611/612
32SE/16D-Channel VME A/D-D/A Boards

FEATURES

- **Two models of VMEbus-based boards**
  DVME-611: 32 single-ended/16 differential A/D channels
  DVME-612: 32 single-ended/16 differential A/D channels and 2 D/A channels
- **Choice of A/D bits/speed**
  12 bits/2, 4, or 20 µSec.
  14 bits/4 µSec.
  16 bits/35 µSec.
- **Four input voltage ranges available: ±10V, ±5V, 0 to +5V, and 0 to +10V dc**
- **Three types of output coding:**
  Bipolar 2's complement
  Bipolar offset binary
  Unipolar straight binary
- **Up to 400 KHz throughput with a *fast throughput mode* for high-speed data transfers (single channel)**
- **On-board interrupt vector register for host system's service routines**
- **80 dB CMRR at gain of 128**
- **Two TTL digital outputs**



- **Eight-stage programmable gain amplifier (PGA)**
- **±0.05% full-scale range accuracy for D/A channels**
- **Channel expansion boards for up to 256 channels**
  DVME-641: Non-isolated, high-level inputs
  DVME-643: Isolated, thermocouple, RTD, high-level, 4-to-20 mA inputs
  DVME-645: Simultaneous sample/hold inputs

GENERAL DESCRIPTION

The DVME-611/612 are DATEL's VMEbus based high-end A/D conversion boards. The A/D boards provide up to 16-bit binary data from up to 32 single-ended or 16 differential analog input channels. DATEL also offers optional expansion boards for up to 256 single-ended or differential analog input channels. The DVME-612 is also equipped with two D/A channels, operable in four output voltage ranges.

The on-board hardware essentially consists of multiplexers, a PGA, an A/D converter, and registers. The PGA is programmable for gains from 1 to 128 in binary increments. Both the DVME-611 and the DVME-612 are available in several models depending upon the A/D converter module used. The A/D converter modules are easily field-replaceable. All models except the DVME-611D and the DVME-612D contain a sample/hold amplifier.

The host-programmable command register controls the A/D conversion process. Depending upon the contents of the command register, an external trigger may also initiate the A/D conversion process. The host system may obtain information pertaining to the A/D conversion and control selections by reading the status register.

The channel and control information from the channel select logic section is brought out to the J4 expansion connector. The control lines include End of Conversion (EOC), End of Scan (EOS), settling time delay, and external trigger signals. These control signals on the expansion connector are also usable with externally multiplexed input channels. The host system selects the start and final channels for the A/D scanning process.

The analog output section on the DVME-612 offers ±1/2 LSB differential non-linearity and operates at ±0.05% of full-scale range accuracy.

Functionally, the analog signal from the input channel is amplified and converted into binary data. The resolution depends on the A/D converter module used. Figure 1 is a functional block diagram of the DVME-611/612 A/D boards. Data from the A/D converter module is coded via jumpers into straight binary, offset binary, or 2's complement coding. The binary A/D data is transferred to the host system through the VMEbus transceivers.

The DVME-611/612 A/D boards can operate in a *fast throughput mode* for applications requiring fast data transfers. This mode is selectable using the command register. The *fast throughput mode* guarantees transfer of A/D data on to the VMEbus without having to test the conversion status. When A/D data is read, this mode delays the host CPU DTACK✻ while EOC = 0.

The DVME-611/612 A/D boards come with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the A/D boards. The user's manual also contains information on troubleshooting the boards

The boards are shipped with a 5.25 inch MS-DOS disk containing an example source program. Consult the factory regarding the availability of the diagnostic program's source code in other disk formats.

VME Interface

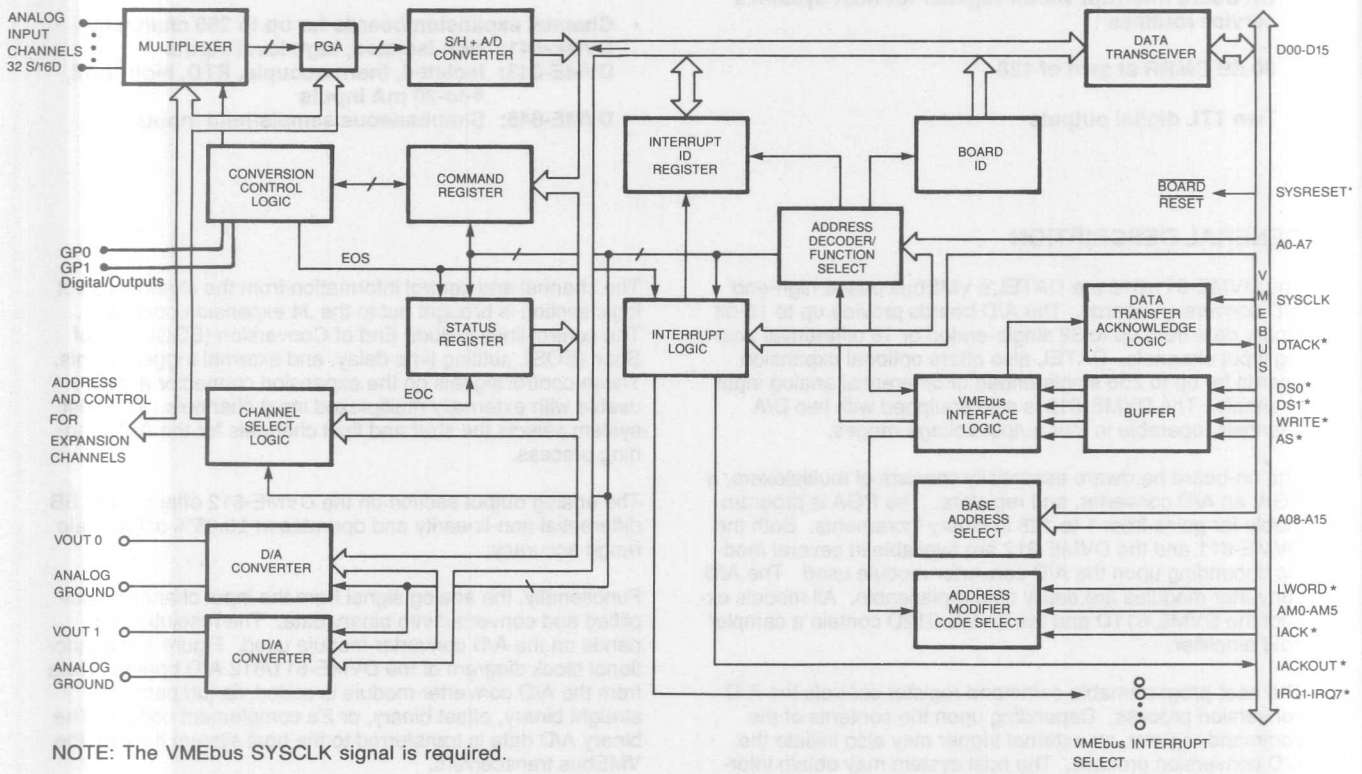
The DVME-611/612 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes.

The DVME-611/612 generates the data acknowledge (DTACK✻) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK✻ signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes VMEbus control lines (WRITE✻, DS0✻, DS1✻, and AS✻) to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-611/612 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

VMEbus Interrupt Logic

The interrupt logic section senses an EOC or EOS condition and generates an interrupt request on one of the VMEbus interrupt lines (IRQ1✻ through IRQ7✻). The interrupt lines are jumper-selectable. The interrupt logic accepts IACK✻ and IACKIN✻ signals from the host system as interrupt acknowledge and daisy chain input signals. Depending upon the interrupt level, the on-board logic loads the interrupt ID number on to the VMEbus or generates the daisy chain IACKOUT✻ signal.



NOTE: The VMEbus SYSCLK signal is required.

Figure 1. DVME-611/612 Functional Block Diagram

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FUNCTIONAL SPECIFICATIONS

(Typical at 25 °C, unless otherwise noted)

VMEbus INTERFACE

Data Bus ..... 16 Bits. (A16:D16 slave)
Address Bus..... Short I/O Space 16 address lines
Address Modifier Codes.. Codes used 29H, 2DH, 39H, and 3DH
Interrupts ..... 1 line, jumper-selectable
2 interrupt ID's for EOC and EOS
Software programmable
Memory Mapping ..... Short I/O space, user or supervis-
or 256 words allocated per board
Data Transfer..... DTACK✱ signal line
Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines

ANALOG INPUT

Number of Channels..... 32 single-ended or 16 differential
Channel Expansion..... 256 single-ended or differential; requires external multiplexing. Use DATEL's DVME-641, DVME-643, or DVME-645 mux boards.
Input Configuration..... Single-ended or differential
Input Ranges ..... ±10V, ±5V, 0 to +5V, or
0 to +10V, jumper-selectable.
See Table 2.
Digital Outputs
Standard..... Offset binary
Jumperable ..... Straight binary or 2's complement
External Start Trigger ..... TTL compatible, negative going edge.
Minimum pulse width = 100 nS
Maximum pulse width = 2 µS
Common Mode Voltage... ±10V dc, maximum, non-isolated
Input Bias Current..... 8 nA, maximum
Over Voltage Protection.. ±35V dc, maximum
Input Impedance
Differential to ground ..... 10 megohms, minimum

PERFORMANCE

Programmable Gain..... Uses an AM-543MC for gains of X1, X2, X4, X8, X16, X32, X64, X128
Common Mode Rejection for ±10V input signal at 60 Hz, minimum ..... 75 dB at a gain of 2
80 dB at a gain of 128
Full-Scale Range Accuracy, minimum
DVME-611A/612A..... 0.025% at a gain of 1
DVME-611E/612E..... 0.20% at a gain of 128
DVME-611B/612B..... 0.05% at a gain of 1
0.20% at a gain of 128
DVME-611C/612C..... 0.010% at a gain of 1
0.20% at a gain of 128
DVME-611D/612D..... 0.0063% at a gain of 1
0.20% at a gain of 128
DVME-611F/612F ..... 0.01% at a gain of 1
PGA plus MUX Settling Time, maximum..... 8 µS at a gain of 1
12 µS at a gain of 16
40 µS at a gain of 64
100 µS at a gain of 128

Min. conversion time
DVME-611A/612A..... 20 µS at a gain of 1
110 µS at a gain of 128
DVME-611B,E/612B,E... 8 µS at a gain of 1
102 µS at a gain of 128
DVME-611C/612C..... 35 µS at a gain of 1
110 µS at a gain of 128
DVME-611D/612D..... 400 mS at a gain of 1
400 mS at a gain of 128
DVME-611F/612F ..... 4 µS at gain = 1

Note: Allow 20 minutes warm-up for DVME-611F/612F

Resolution and Throughput

(Scan Mode)	Resolution in bits	Conversion time	Throughput conversions /sec.*
DVME-611A/612A	12	20 µS	40,320
DVME-611B/612B	12	4 µS	160,000
DVME-611C/612C	16	35 µS	18,667
DVME-611D/612D	16	400 mS	2.5
DVME-611E/612E	12	2 µS	see notes
DVME-611F/612F	14	4 µS	100,000

*Typical sample rate per channel in scan mode.

Temperature Drift and Linearity

Model	Gain Temperature Coefficient (ppm/ °C)	Zero Temperature Drift, (ppm/ °C)	Linearity Error
DVME-611A/612A	±20	20	1/2 LSB
DVME-611B/612B	±20	20	1/2 LSB
DVME-611C/612C	±20	20	2 LSB
DVME-611D/612D	±10	10	2 LSB
DVME-611E/612E	±20	±20	1/2 LSB
DVME-611F/612F	±15	±15	2 LSB

Optional Multiplexer Expansion Boards

Model	Number of expansion channels Single-ended	Differential	Input type
DVME-641	32	16	High-level, non-isolated
DVME-643T	–	8	Thermocouple Isolated
DVME-643H	–	8	High-level Isolated
DVME-645	16	8	Simultaneous Sample/Hold high-level non-isolated

ANALOG OUTPUT (For DVME-612 models only)

Number of Channels 2
Output Range ..... ±10V, ±5V, 0 to +5V, or 0 to +10V
Digital Input Coding ..... Bipolar 2's complement, bipolar offset binary or unipolar straight binary
Resolution ..... 12 Bits, bits D0 through D3 not used
Reset ..... Minus, full-scale, -10V for 2's complement and offset binary 0V for Unipolar
Full-Scale Range
Accuracy ..... .05%, minimum
Diff. Non-Linearity ..... 0.5 LSB, minimum
Zero Temperature Drift ..... 5 ppm/ °C, maximum
Offset Temperature Drift .. 20 ppm/ °C, maximum
Gain Temperature Drift .... 20 ppm/ °C, maximum
Settling Time ..... 10 µS, maximum
Output Current ..... 5 milliamps, maximum
Output Impedance ..... 50 milliohms, typical

POWER SUPPLY REQUIREMENTS

+5V dc ±5% at 2.5 Amperes
Note: On-board dc-to-dc converter generates ±15V dc for the DVME-611/612 logic circuits

CONNECTORS

VMEbus P1 connector ..... 96-pin male DIN connector
J1 and J2 Analog Input Connectors ..... 25-pin D-type female connectors
J3 Analog Output Connector ..... 9-pin D-type female connector
J4 Analog Expansion Connector ..... 25-pin D-type female connector

PHYSICAL-ENVIRONMENTAL

Outline Dimensions ..... 9.19"W x 6.3"D x 0.6"H (233.5 x 160 x 15.24 mm)
Weight ..... 1 lb. 0.5 oz. (467.8 grams)
Operating Temp. Range ... 0 to +60 °C
Storage Temp. Range ..... -20 to +80 °C
Relative Humidity ..... 0 to 90%, non-condensing

DVME-611/612 Programming Information

The DVME-611/612 A/D boards use ten registers for data acquisition and control purposes. Table 1 lists the DVME-611/612 registers and their base address offsets. These registers are addressable locations in the host system's address space.

Address	Function	Contents
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification
Base + 128	Write	Command register (80h)
Base + 128	Read	Status register (80h)
Base + 130	Write	Interrupt ID register (82h)
Base + 132	Write	EOC/EOS F/F Reset (84h)
Base + 134	Write	Gain register (86h)
Base + 136	Write	Start channel register (88h)
Base + 136	Read	Current channel register
Base + 138	Write	Final channel register (8Ah)
Base + 140	Write	Start conversion register (8Ch)
Base + 140	Read	A/D data register
Base + 142	Read	Status register (8Eh)
Base + 160	Write	D/A channel 0 (A0h)
Base + 162	Write	D/A channel 1 (A2h)

Table 1. DVME-611/612 Hardware Register Functions

Command Register

The DVME-611/612 boards scan their selected channels under control of the 16-bit command register. Programming the command register selects the modes for starting conversion, calibration, and fast throughput. This register also enables the interrupt, channel address auto-increment, and channel re-scan capabilities. Figure 2 shows the command register format.

Status Register

The DVME-611/612 status register indicates conditions relating to conversion status, channel scanning information, and modes selected. Figure 3 shows the status register format.

Total System Throughput

Total sample-to-sample throughput rate depends on the A/D-S/H settling and conversion period and the user's software period. During the software interval, data is transferred to the host and the next A/D conversion is started. By combining fast throughput mode (DTACK✻ EOC holdoff) with convert-on-read-data, throughput over 400 KHz may be achieved for gain = 1 in single channel mode for model DVME-611E. Data transfer and host memory pointer management may partially overlap A/D Conversion by using the convert-on-read mode.

Fast Throughput Mode

This mode holds off response of the DTACK✻ VMEbus signal with the simultaneous ANDing of three conditions: command register bit 5 = 1, EOC = 0, and a host read of the A/D data register. While DTACK✻ is held off, the host CPU executes wait states. When A/D conversion finishes, EOC = 1 and DTACK✻ is released. Normally the attempted A/D data read now completes, and data is transferred without any EOC polling. Fast throughput should be used with caution since the host must be completely dedicated to A/D data acquisition.

Table 2. A/D Full Scale Input Ranges (PGA gain = 1)

Input Range	Model 611/612A	611/612B,E	611/612C	611/612D	611/612F
0 to +5V	X	NA	NA	NA	NA
0 to +10V	X	X	NA	NA	S
±5V	X	NA	X	NA	S
±10V	X	X	X	X	X

X = supplied, NA = not available, S = solderable on module

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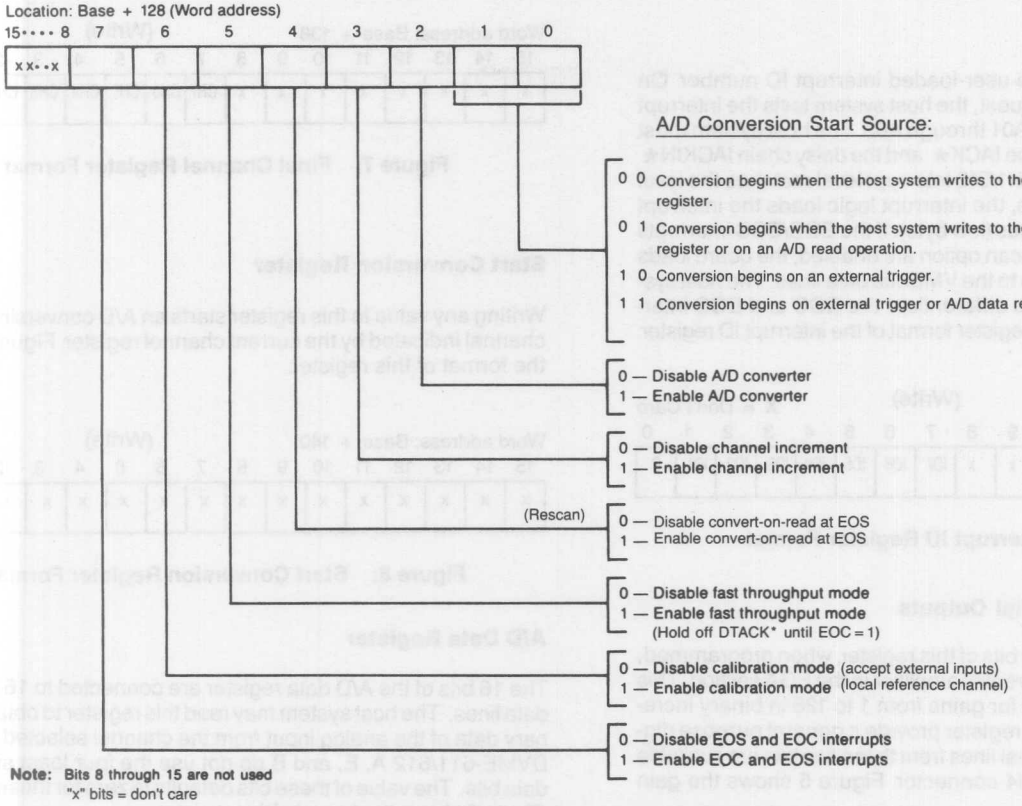


Figure 2: DVME-611/612 Command Register Format (WRITE)

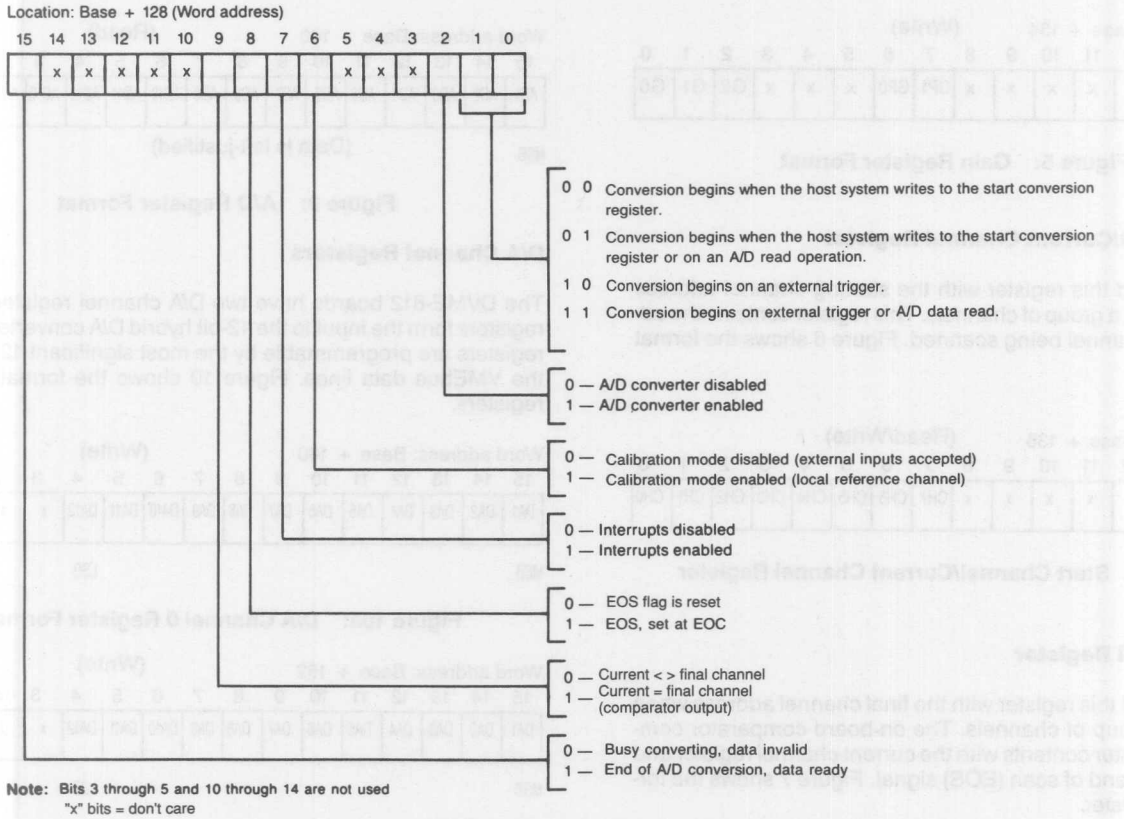


Figure 3: DVME-611/612 Status Register Format (READ)

Interrupt ID Register

This register contains the user-loaded interrupt ID number. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK★ and the daisy chain IACKIN★ signal lines. If the DVME-611/612 interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number on to the VMEbus (low byte). If the EOC/EOS interrupts and the multiple channel scan option are enabled, the board loads the ID number plus one on to the VMEbus data lines. The host system may use these ID's to differentiate the EOC and EOS interrupts. Figure 4 shows the register format of the interrupt ID register.

Word address: Base + 130 (Write) X = Don't Care

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	ID7	ID6	ID5	ID4	ID3	ID2	ID1	0

Figure 4: Interrupt ID Register Format

Gain Register and Digital Outputs

The least three significant bits of this register, when programmed, assign the gain to the differential amplifier in the PGA section. This register is programmable for gains from 1 to 128 in binary increments. Bits 6 and 7 of this register provide a general purpose digital output. The output signal lines from these two bits are available on pins 18 and 6 of the J4 connector. Figure 5 shows the gain register format.

Word address: Base + 134 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	GP1	GP0	x	x	x	G2	G1	G0

Figure 5: Gain Register Format

Start Channel/Current Channel Register

User must load this register with the starting channel address when scanning a group of channels. This register contains the address of the channel being scanned. Figure 6 shows the format of this register.

Word address: Base + 136 (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Figure 6: Start Channel/Current Channel Register

Final Channel Register

User must load this register with the final channel address when scanning a group of channels. The on-board comparator compares this register contents with the current channel register and generates the end of scan (EOS) signal. Figure 7 shows the format of this register.

Word address: Base + 138 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Figure 7: Final Channel Register Format

Start Conversion Register

Writing any value to this register starts an A/D conversions on the channel indicated by the current channel register. Figure 8 shows the format of this register.

Word address: Base + 140 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Figure 8: Start Conversion Register Format

A/D Data Register

The 16 bits of the A/D data register are connected to 16 VMEbus data lines. The host system may read this register to obtain the binary data of the analog input from the channel selected. Models DVME-611/612 A, E, and B do not use the four least significant data bits. The value of these bits defaults to zero for these models. Figure 9 shows the format of this register.

Word address: Base + 140 (Read)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13	AD14	AD15	AD16

MSB (Data is left-justified) LSB

Figure 9: A/D Register Format

D/A Channel Registers

The DVME-612 boards have two D/A channel registers. These registers form the input to the 12-bit hybrid D/A converters. These registers are programmable by the most significant 12 bits from the VMEbus data lines. Figure 10 shows the format of these registers.

Word address: Base + 160 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x

MSB LSB

Figure 10a: D/A Channel 0 Register Format

Word address: Base + 162 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x

MSB LSB

Figure 10b: D/A Channel 1 Register Format

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EOC/EOS F/F Register

Writing any value to this register resets the EOC/EOS flip-flops. Figure 11 shows the format of this register.

Word address: Base + 132 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Figure 11: EOC/EOS F/F Register Format

(These F/F's are also reset by the next start of conversion or by reading A/D data.)

I/O Connections

The DVME-611/612 A/D boards use the J1 and J2 connectors for analog input connections and the J4 connector for channel expansion. The DVME-612 uses the J3 connector for analog output connections. Tables 2, 3, 4, and 5 list the I/O signals of the J1, J2, J3, and J4 connector respectively.

Table 3. DVME-611/612 Analog Input Connector - J1

PIN #	CONFIGURATION	
	SINGLE-ENDED	DIFFERENTIAL
24	CHANNEL 0 IN	CHANNEL 0 HIGH
12	CHANNEL 16 IN	CHANNEL 0 LOW
25	ANALOG RETURN	ANALOG RETURN
10	CHANNEL 1 IN	CHANNEL 1 HIGH
23	CHANNEL 17 IN	CHANNEL 1 LOW
11	ANALOG RETURN	ANALOG RETURN
21	CHANNEL 2 IN	CHANNEL 2 HIGH
9	CHANNEL 18 IN	CHANNEL 2 LOW
22	ANALOG RETURN	ANALOG RETURN
7	CHANNEL 3 IN	CHANNEL 3 HIGH
20	CHANNEL 19 IN	CHANNEL 3 LOW
8	ANALOG RETURN	ANALOG RETURN
18	CHANNEL 4 IN	CHANNEL 4 HIGH
6	CHANNEL 20 IN	CHANNEL 4 LOW
19	ANALOG RETURN	ANALOG RETURN
4	CHANNEL 5 IN	CHANNEL 5 HIGH
17	CHANNEL 21 IN	CHANNEL 5 LOW
5	ANALOG RETURN	ANALOG RETURN
15	CHANNEL 6 IN	CHANNEL 6 HIGH
3	CHANNEL 22 IN	CHANNEL 6 LOW
16	ANALOG RETURN	ANALOG RETURN
1	CHANNEL 7 IN	CHANNEL 7 HIGH
14	CHANNEL 23 IN	CHANNEL 7 LOW
2	ANALOG RETURN	ANALOG RETURN

Table 4. DVME-612 Analog Output Connector - J3

PIN #	SIGNAL LINE
1	CHANNEL 0 VOUT
6	ANALOG RETURN
4	CHANNEL 1 VOUT
9	ANALOG RETURN

Table 5. DVME-611/612 Analog Input Connector - J2

PIN #	CONFIGURATION	
	SINGLE-ENDED	DIFFERENTIAL
24	CHANNEL 8	CHANNEL 8 HIGH
12	CHANNEL 24	CHANNEL 8 LOW
25	ANALOG RETURN	ANALOG RETURN
10	CHANNEL 9	CHANNEL 9 HIGH
23	CHANNEL 25	CHANNEL 9 LOW
11	ANALOG RETURN	ANALOG RETURN
21	CHANNEL 10	CHANNEL 10 HIGH
9	CHANNEL 26	CHANNEL 10 LOW
22	ANALOG RETURN	ANALOG RETURN
7	CHANNEL 11	CHANNEL 11 HIGH
20	CHANNEL 27	CHANNEL 11 LOW
8	ANALOG RETURN	ANALOG RETURN
18	CHANNEL 12	CHANNEL 12 HIGH
6	CHANNEL 28	CHANNEL 12 LOW
19	ANALOG RETURN	ANALOG RETURN
4	CHANNEL 13	CHANNEL 13 HIGH
17	CHANNEL 29	CHANNEL 13 LOW
5	ANALOG RETURN	ANALOG RETURN
15	CHANNEL 14	CHANNEL 14 HIGH
3	CHANNEL 30	CHANNEL 14 LOW
16	ANALOG RETURN	ANALOG RETURN
1	CHANNEL 15	CHANNEL 15 HIGH
14	CHANNEL 31	CHANNEL 15 LOW
2	ANALOG RETURN	ANALOG RETURN

Table 6. DVME-611/612 Expansion Connector - J4

PIN #	SIGNAL LINE
13	EXTERNAL CHANNEL ADDRESS 0 OUT
25	EXTERNAL CHANNEL ADDRESS 1 OUT
12	EXTERNAL CHANNEL ADDRESS 2 OUT
24	EXTERNAL CHANNEL ADDRESS 3 OUT
11	EXTERNAL CHANNEL ADDRESS 4 OUT
23	EXTERNAL CHANNEL ADDRESS 5 OUT
10	EXTERNAL CHANNEL ADDRESS 6 OUT
22	EXTERNAL CHANNEL ADDRESS 7 OUT
16	DIGITAL GROUND
9	EXTERNAL CHANNEL ADDRESS VALID OUT
8	START CONVERSION STROBE OUT
20	SETTLING DELAY* IN
7	END OF CONVERSION OUT
19	END OF SCAN OUT
17	EXTERNAL TRIGGER IN*
18	GENERAL PURPOSE OUTPUT 0
6	GENERAL PURPOSE OUTPUT 1
4	DIGITAL GROUND
21	RESERVED
5	RESERVED
1	EXTERNAL ANALOG LOW IN
14	EXTERNAL ANALOG HIGH IN
2, 15	ANALOG COMMON
3	+5V dc REFERENCE OUT (5mA)

DVME-611/612 Board Indentification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+3	M	This ASCII code is present
+5	E	for all DATEL VMEbus boards
+7	I	
+9	D	
+0B	D	Manufacturer ID
+0D	A	DAT is the ID for DATEL
+0F	T	
+11	d	Board model number
+13	V	
+15	M	
+17	E	
+19	–	
+1B	6	
+1D	1	
+1F	1 or 2	

ORDERING INFORMATION

DVME-611 (A/D only)
DVME-612 (A/D + D/A)

- A - 12-bit/20 µS ADC
- B - 12-bit/4 µS ADC
- C - 16-bit/35 µS ADC
- D - **DISCONTINUED***
- E - 12-bit/2 µS ADC
- F - 14-bit/4 µS

Optional Multiplexer Expansion Boards

DVME-641 - 32S/16D Channel high-level non-isolated inputs.
DVME-643 - 8D Channel isolated inputs.
DVME-645 - 16S/8D Channel simultaneous sample/hold high-level non-isolated inputs.

***DVME-611D and -612D are discontinued. Use DVME-611C and -612C instead.**

Each board includes a disk and manual.

DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base +64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	Not used	
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended; 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples, RTD's, strain gages, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	Not used	
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board
Base + 176 through Base + 191	Not used	
Base + 192 through Base + 255	Not used	

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DVME-613
Isolated, Industrial 16SE or 8D-Channel VME A/D Board

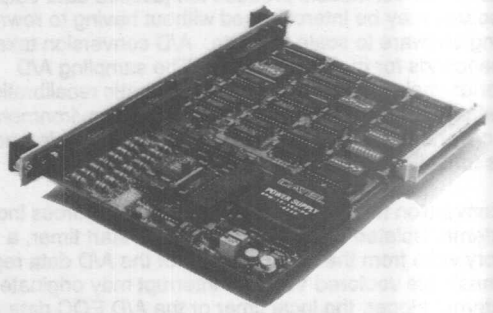
FEATURES

- **16 single-ended or 8 differential analog input channels**
- **12, 14, or 16-bit A/D resolution**
- **Isolation to ±500V**
- **On-board programmable gain amplifier and start timer**
- **8 in and 8 out discrete digital lines**
- **Programmable vectored VME interrupt**
- **Simple programming for any operating system or language**

GENERAL DESCRIPTION

Designed for industrial data acquisition, process control, and factory automation, the DVME-613 is a cost-effective isolated analog input board for VMEbus computers. The DVME-613 will accept sixteen single-ended or eight differential input channels which are all isolated from the VMEbus by ±500V. In addition, each channel is protected from adjacent channel overloads up to ±150 Volts. The common mode voltage range is ±11 Volts relative to isolated analog ground.

The analog input range is selectable as ± 10 Volts for bipolar inputs or 0 to +10 Volts unipolar. By using an on-board programmable gain amplifier (PGA), inputs may be accepted directly from bridges, load cells, RTD's, and strain gauges. The PGA includes selectable gain ranges of times one, ten and one hundred for low level inputs.



An optional signal conditioning pad area accepts shunt resistors, attenuators, hash filters, and clamps. This allows direct input from isolated 1-5mA or 4-20mA transmitters and from voltage sources greater than ± 10 Volts full scale. For bridge-type sensors, on-board regulated DC excitation voltage is provided which is fully isolated from VMEbus.

The DVME-613 inputs are plug compatible with DATEL's DVME-691 rack-mount signal conditioning panel for screw terminal inputs. Three A/D converter options are offered. The DVME-613A is a 12-bit A/D converter with overall accuracy of ±0.05% of full scale. Resolution of the DVME-613A is 2.5mV per count for unipolar inputs.

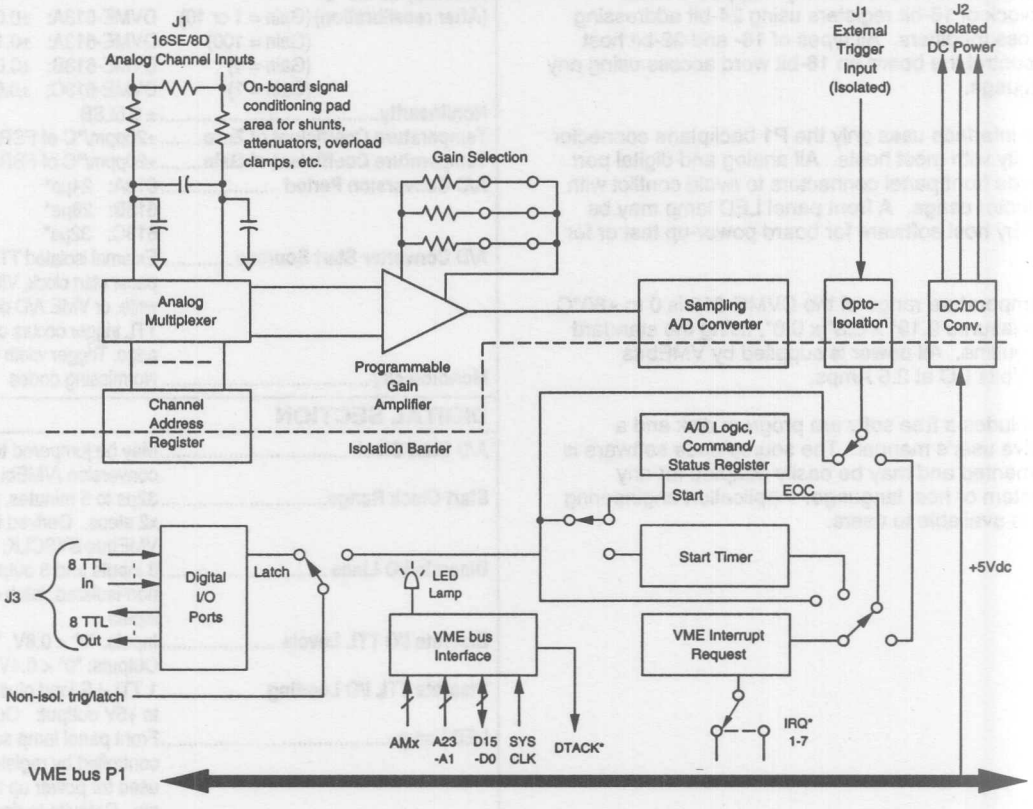


Figure 1. DVME-613 Simplified Block Diagram

GENERAL DESCRIPTION (Cont.)

The DVME-613B offers a 14-bit A/D converter and for highest resolution inputs, a 16-bit converter is included on the DVME-613C. All models produce left-justified data outputs so that boards may be interchanged without having to rewrite existing software to scale the data. A/D conversion takes 24 microseconds for the DVME-613A. The sampling A/D converter design offers continuous automatic recalibration. To insure reliability in industrial process control environments, local channels may be dedicated to ground and reference inputs for self-testing of signal paths.

A/D conversion may be started from several sources including an external isolated trigger input, the local start timer, a memory write from the host or a read of the A/D data register. The maskable vectored VMEbus interrupt may originate from an external trigger, the local timer or the A/D EOC data ready signal.

VMEbus interrupts are fully vectored using selectable IRQ 1-7 levels.

The A/D data ready EOC signal is indicated in a status register and maskable VMEbus interrupt. All modes are software controlled by local command and status registers.

The DVME-613 provides 16 digital lines for logic control of devices such as pumps, heaters and valves. These lines are TTL logic compatible and arranged as eight inputs and eight outputs. A separate control input latches the eight TTL input lines.

The DVME-613 is a VMEbus SA24:SD16 slave. The board appears to the VMEbus as a memory-mapped 8-word contiguous block of 16-bit registers using 24-bit addressing and six address modifiers. All types of 16- and 32-bit host CPU's may control the board on 16-bit word access using any software language.

The VMEbus interface uses only the P1 backplane connector for compatibility with most hosts. All analog and digital port interfacing uses front panel connectors to avoid conflict with P2 bus connector usage. A front panel LED lamp may be programmed by host software for board power-up test or for alarms.

Operating temperature range of the DVME-613 is 0 to +60°C. The board measures 9.19" x 6.3" x 0.6", using the standard 6U VMEbus outline. All power is supplied by VMEbus requiring +5 Volts DC at 2.5 Amps.

The board includes a free software program disk and a comprehensive user's manual. The source-code software is heavily commented and may be easily adapted for any operating system or host language. Application engineering consultation is available to users.

FUNCTIONAL SPECIFICATIONS

(Specifications are for the total system and are typical at +25°C, gain = 1 unless noted)

ANALOG INPUTS

Number of Channels	8 differential or 16 single-ended	
Full Scale Input Ranges	**Unipolar**	**Bipolar**
Gain = 1	0 to 10V	±10V
Gain = 10	0 to 1V	±1V
Gain = 100	0 to 100mV	±100mV
Input Isolation	±500V max. from analog section to VMEbus	
Isolation Capacitive Coupling	25pF analog section to VME	
Isolation Resistive Coupling	100MΩ analog to VME	
Common Mode Voltage Range	± 11V to isolated ground	
Common Mode Rejection	86 dB, dc to 60 Hz, gain = 100, 1kΩ source unbalance	
Channel-to-Channel Protection	±150V max. sustained	
Input Bias Current	±200 picoamps	
Input Impedance (power on)	100MΩ to isolated ground	
Input Impedance (power off)	33kΩ to isolated ground	
Programmable Gain Amplifier	Jumper selectable for gains of 1, 10, or 100. Will accept precision resistor for user defined gain	
PGA Settling Delay	10µs, gain = 1 (after channel selection); 20µs, gain = 10; 100µs, gain = 100	
A/D Output Resolution	12 binary bits (DVME-613A) 14 binary bits (DVME-613B) 16 binary bits (DVME-613C)	
A/D Output Coding	Selectable as unipolar straight binary or bipolar offset binary	
Accuracy at +25° C		
(After recalibration)	(Gain = 1 or 10)	DVME-613A: ±0.05% of FSR
	(Gain = 100)	DVME-613A: ±0.1% of FSR
	(Gain = 1)	DVME-613B: ±0.0125% of FSR
	(Gain = 1)	DVME-613C: ±0.0075% of FSR
Nonlinearity	± 0.5LSB	
Temperature Coefficient of Zero	±20ppm/°C of FSR	
Temperature Coefficient of Gain	±20ppm/°C of FSR	
A/D Conversion Period	613A: 24µs* 613B: 28µs* 613C: 32µs*	
A/D Converter Start Sources	External isolated TTL trigger, local pacer start clock, VME command write, or VME A/D data read. The TTL trigger occurs on the rising edge. Trigger width 0.1 to 5µs	
Monotonicity	No missing codes	

DIGITAL SECTION

A/D Start Clock	May be jumpered to start an A/D conversion /VMEbus interrupt
Start Clock Range	32µs to 5 minutes, jumperable in x2 steps. Derived from 16MHz VMEbus SYSCLK.
Discrete I/O Lines	8 inputs and 8 outputs, non-isolated, latch control for inputs
Discrete I/O TTL Levels	Inputs: "0" < 0.8V, "1" > 2.0V Outputs: "0" < 0.4V, "1" > 2.4V
Discrete TTL I/O Loading	1 TTL-LS load plus 4.7kΩ pullup to +5V outtput: Output: 24mA
LED Lamp	Front panel lamp software controlled by register bit. May be used for power up test, alarms, etc. Defaults to dark at power up or bus reset.

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VMEbus INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Architecture	SAD24:SD16 slave consisting of 8 contiguous word registers.
Data Bus Width	16 bits using P1 connector.
Address Bus	24 address lines (A23-A1) plus 6 Address Modifiers.
Address Modifier Codes	39 or 3D hex, selectable
VMEbus Interrupt	1 line, selectable IRQ 1-7*. Asserts maskable programmable 8-bit vector ID code.
Interrupt Source	Selectable from external trigger, start timer or A/D data ready.
Data Transfer	Uses 16 MHz VMEbus SYSCLK signal to generate DTACK* signal with selectable delay.

CONNECTORS	
VMEbus, P1	96-pin male DIN connector. The P2 connector is not used.
Local Isolated Analog Input and Isolated Trigger	J1 connector, 25-pin DB-25S female on front panel, pin-compatible to DVME-691 screw terminator.
Isolated DC Power	J2 connector, 25-pin DB-25S female on front panel. Power available: ±15V dc at 25mA max.
Discrete Digital I/O	J3 connector, 25-pin DB-25S female on front panel.

MISCELLANEOUS	
Power Required	+5V dc ±5% at 2.5 Amps max. from VMEbus.
Operating Temperature Range	0 to +60°C
Storage Temperature Range	-20 to +80°C
Relative Humidity	10 to 90%, non-condensing
Altitude	0 to 10,000 feet.
Outline Dimensions	Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233,5 x 160 x 15,24 mm)
Weight	17 ounces (482 grams)

*Single channel conversion rates are shown. For multichannel inputs, an additional 20 µs must be allowed after channel selection before the next A/D conversion start.

TYPICAL BRIDGE-TYPE INPUT CONNECTIONS

Figure 2 shows the DVME-613 connected to a bridge-type transducer. Notice that the bridge excitation is derived from the +15V dc power available from the DVME-613. The excitation voltage is regulated.

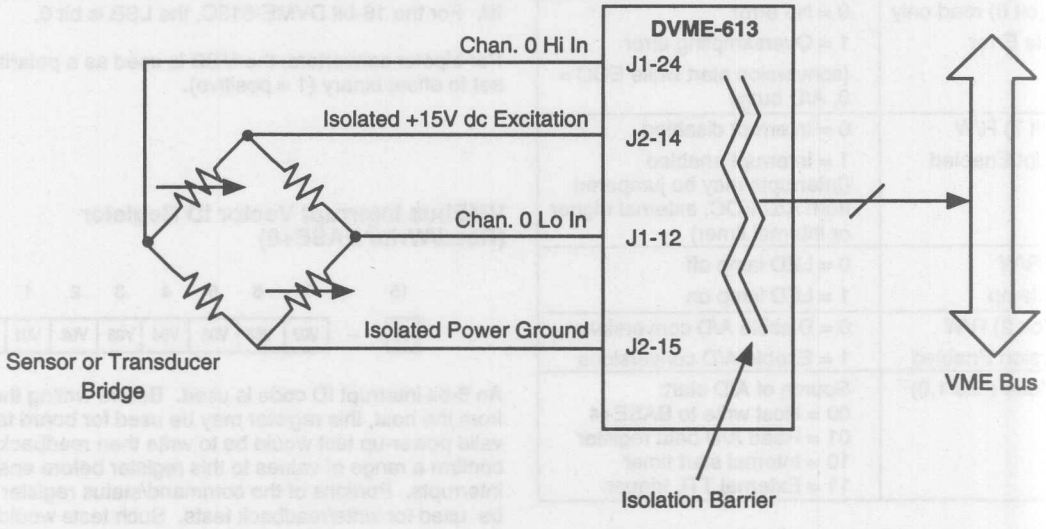


Figure 2. Typical Bridge-type Input Connections

REGISTER PROGRAMMING

Register Memory Mapping

BASE address switches must be selected for even address boundaries. All registers must be accessed on 16-bit word memory operations.

Address (Hex)	Direction	Description
BASE+0	Write	Command register
BASE+0	Read	Status register
BASE+2	Write	Channel address register
BASE+4	Write	Start A/D conversion register
BASE+6	Read	A/D data register
BASE+8	Write	Interrupt vector ID register
BASE+8	Read	Interrupt vector ID register
BASE+A	Write	Calibrate A/D converter
BASE+C	Write	TTL digital output port register
BASE+E	Read	TTL digital input port register

Command/Status Register (Write/Read BASE+0)

15	--	8	7	6	5	4	3	2	1	0
EOC	--	OVR SMP	INT ENB	LED ON	X	X	X	CNV ENB	Start Mode	

("x" bits are don't care or not defined)

If interrupt is not used, the host should poll EOC before reading A/D data. The read of the A/D data register resets EOC to 0 even if another conversion is not started.

EOC (bit 15) read only End of A/D Conversion	0 = Conversion in progress. Data not valid 1 = Conversion done. Data ready
OVR SMP (bit 8) read only Over Sample Error	0 = No error 1 = Oversampling error (conversion start while EOC = 0, A/D busy)
INT ENB (bit 7) R/W VME Interrupt Enabled	0 = Interrupt disabled 1 = Interrupt enabled (Interrupts may be jumpered from A/D EOC, external trigger or internal timer)
LED (bit 6) R/W Front panel lamp	0 = LED lamp off 1 = LED lamp on
CNV ENB (bit 2) R/W A/D Conversion Enabled	0 = Disable A/D conversions 1 = Enable A/D conversions
A/D Start Mode (bits 1,0) R/W	Source of A/D start: 00 = Host write to BASE+4 01 = Read A/D data register 10 = Internal start timer 11 = External TTL trigger

Program the command register last. All registers default to zeroes at power-up.

Channel Address Register (Write BASE+2)

15	--	7	6	5	4	3	2	1	0
X	--	GP1	GP0	X	X	Chn Adr 3	Chn Adr 2	Chn Adr 1	Chn Adr 0

GP1, GP0 (bits 7,6) - These are spare unassigned register output bits available for any purpose. They appear at integrated circuit U19-10,12.

Chn Adr (bits 3-0) - Channel Address input corresponding to A/D channels 0 through 7 (differential) or 0 through 15 (single-ended).

Start A/D Conversion Register (Write BASE+4)

15	--	7	6	5	4	3	2	1	0
X	--	X	X	X	X	X	X	X	X

An A/D conversion may be started by a write to this register if enabled by the command register mode 00. EOC will be set to 0 after conversion is started and until data is ready.

A/D Data Register (Read BASE+6)

15	--	7	6	5	4	3	2	1	0
MSB ALL	--				LSB 12		LSB 14		LSB 16

A/D data is left justified for all converters. The least significant bit for the 12-bit DVME-613A is bit 4 with bits 3-0 filled with zeroes. The LSB for the 14-bit DVME-613B is bit 2 with zero fill. For the 16-bit DVME-613C, the LSB is bit 0.

For bipolar converters, the MSB is used as a polarity bit and is set to offset binary (1 = positive).

VMEbus Interrupt Vector ID Register (Read/Write BASE+8)

15	--	7	6	5	4	3	2	1	0
X	--	V07	V06	V05	V04	V03	V02	V01	V00

An 8-bit interrupt ID code is used. Before writing the ID code from the host, this register may be used for board testing. A valid power-up test would be to write then readback and confirm a range of values to this register before enabling interrupts. Portions of the command/status register may also be used for write/readback tests. Such tests would confirm the bus interface and register logic. Further testing may be done using the dedicated reference inputs to the A/D converter. If all tests succeed, the front panel LED lamp may be lit.

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Calibrate A/D Converter (Write BASE+A)

15		7	6	5	4	3	2	1	0
X	--	X	X	X	X	X	X	X	X

Writing to this register will start an A/D calibration cycle for approximately 320 milliseconds until EOC. This operation should be done once after power up. During calibration, the A/D converter makes internal corrections. Periodic calibration is optional in stable temperature environments but is suggested frequently with changing temperatures.

Discrete Digital Output Register (Write BASE+C)

15		7	6	5	4	3	2	1	0
X	--	D07	D06	D05	D04	D03	D02	D01	D00

Discrete Digital Input Register (Read BASE+E)

15		7	6	5	4	3	2	1	0
X	--	D07	D06	D05	D04	D03	D02	D01	D00

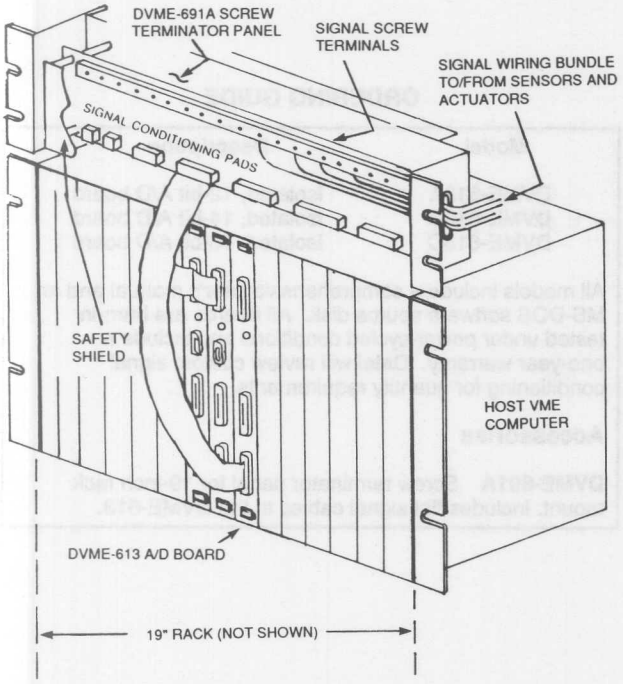


Figure 3. Cabling the DVME-613 Using DATEL's DVME-691 Screw Terminator Panel

FRONT PANEL INPUT/OUTPUT CONNECTIONS

Pin numbering is shown as viewed from the front panel.

Discrete Non-Isolated Digital I/O - Connector J3

Digital Out 7	25	13	External Trig*/ Latch In
Digital Out 6	24	12	Digital Ground
Digital Ground	23	11	Digital Out 5
Digital Out 3	22	10	Digital Out 4
Digital Out 2	21	9	Digital Ground
Digital Ground	20	8	Digital Out 1
Digital In 7	19	7	Digital Out 0
Digital In 6	18	6	Digital Ground
Digital Ground	17	5	Digital In 5
Digital In 3	16	4	Digital In 4
Digital In 2	15	3	Digital Ground
Digital Ground	14	2	Digital In 1
		1	Digital In 0

Isolated DC Power Out - Connector J2

Non-Isol. Dig. Ground	25	13	Non-Isol. Digital Ground
+5V dc Out (non-isol.)	24	12	+5V dc Out (non-isol.)
No Connection	23	11	No Connection
No Connection	22	10	No Connection
No Connection	21	9	No Connection
No Connection	20	8	Spare to internal pad
No Connection	19	7	Spare to internal pad
No Connection	18	6	Spare to internal pad
No Connection	17	5	Spare to internal pad
-15V dc Out (<25 mA)	16	4	No Connection
Isolated Ground	15	3	-15V dc Out (<25mA)
+15V dc Out (<25mA)	14	2	Isolated Ground
		1	+15V dc Out (<25mA)

Isolated Analog Inputs - Connector J1

Signal Ground	25	13	Isol. External Trigger In
Chan. 0 Hi	24	12	Chan. 8 Hi/Chan. 0 Lo
Chan. 9 Hi/Chan. 1 Lo	23	11	Signal Ground
Signal Ground	22	10	Chan. 1 Hi
Chan. 2 Hi	21	9	Chan. 10 Hi/Chan. 2 Lo
Chan. 11 Hi/Chan. 3 Lo	20	8	Signal Ground
Signal Ground	19	7	Chan. 3 Hi
Chan. 4 Hi	18	6	Chan. 12 Hi/Chan. 4 Lo
Chan. 13 Hi/Chan. 5 Lo	17	5	Signal Ground
Signal Ground	16	4	Chan. 5 Hi
Chan. 6 Hi	15	3	Chan. 14 Hi/Chan. 6 Lo
Chan. 15 Hi/Chan 7 Lo	14	2	Signal Ground
		1	Chan. 7 Hi

Channel address notation: Single-ended/Differential

PROGRAMMING

The DVME-613 appears to the host computer as a block of 16-bit memory-mapped registers. To program the DVME-613, read/write memory word operations may be used from any language. In "C", short pointers will access these registers. In 680X0 assembly language, move word (move.w) operations do the job. Since the DVME-613 is addressed as absolute memory, any host language or operating system may be used. In UNIX, a library function may be needed to map absolute physical addresses to logical addresses.

Either polled status bits or interrupts may be used to indicate when A/D data is ready. If you wish to use interrupts, a simple device driver may be used to send a flag to the Operating System. A device driver is not necessary for polled operation.

A sample "C" program to control the DVME-613 is listed below:

```
/* 613c.c demo 4may89 ldc */

#include <stdio.h>
#include <io.h>

#define SAMPLES 8 /* last channel + 1 to scan */

/* The base address below is set by board switches before
installation. Change this base address for your system: */

#define BASPTR 0xFF0000 /* 24-bit address */

/* Make sure all shorts declared below refer to 16-bit words */

unsigned short *base_ptr; /* base address */

/* offsets to board registers: */
unsigned short *ctl_ptr, /* command-status */
   *chan_ptr, /* channel address */
   *start_ptr, /* start conversion */
   *addat_ptr; /* A/D data */

unsigned short outdata[8]; /* array to store A/D samples */
int scan(int samples), channel, wait(int delay);

main(){
    /* initialize pointers to registers.
   Note pointer (cast) */
   base_ptr = (unsigned short *) BASPTR;
   ctl_ptr = (unsigned short *) (BASPTR + 0);
   chan_ptr = (unsigned short *) (BASPTR + 2);
    addat_ptr = (unsigned short *) (BASPTR + 6);

   scan(SAMPLES);
   printf("\nA/D data (hex):");
   for( channel=0 ; channel < SAMPLES ; channel++ )
      printf("\nChan. %d = %x", channel, outdata [channel] );
} /* end of main */

/*   Functions
*/

wait(delay){
while(delay--)
    ;
}
/* Scan()  collects one scan of A/D samples to outdata[ ] with
sequential channel addressing starting at channel 0. */

scan(samples){
    int channel = 0; /* current channel address started at 0 */

   /* Initialize command register, no interrupts, LED on,
   converter enabled, trigger on A/D data read: */
    *ctl_ptr = 0x0045;
    *chan_ptr = 0; /* start at channel 0 */
   wait(10); /* Adjust this for a 20-microsecond minimum set-
tling delay whenever the channel address is changed */

   /* Do one dummy A/D read to start conversion. This sample
will be overwritten: */
   outdata [channel] = *addat_ptr;

   while( channel < samples ) {
      /* wait for EOC true */
      while(( 0x8000 & *ctl_ptr ) != 0x8000 )
         ;
      *chan_ptr = channel + 1; /* bump channel address */
      wait(10); /* settling delay */
      /* store the last channel and start the next one */
      outdata [channel++] = *addat_ptr;
   }
}
```

ORDERING GUIDE

Model	Description
DVME-613A	Isolated, 12-bit A/D board
DVME-613B	Isolated, 14-bit A/D board
DVME-613C	Isolated, 16-bit A/D board

All models include a comprehensive user's manual and an MS-DOS software source disk. All boards are burn-in tested under power-cycled conditions and include a one-year warranty. Datel will review custom signal conditioning for quantity requirements.

Accessories

DVME-691A Screw terminator panel for 19-inch rack mount. Includes flat signal cables to the DVME-613.

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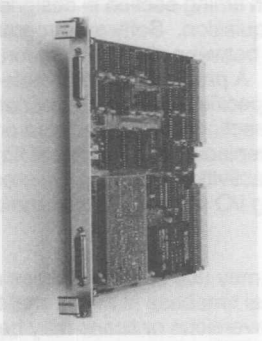
DATEL®
INNOVATION and EXCELLENCE

DVME-614
High-Speed, Analog Input Board for VMEbus Computers

FEATURES

- **Up to 10MHz A/D sample rate**
- **Choice of 12 or 14-bit A/D resolution**
- **Very low harmonic distortion**
- **Optional 2, 4, or 8-channel simultaneous sampling**
- **On-board FIFO memory for up to 16,384 samples**
- **Ideal for FFT's, DSP or array-processor "front ends"**
- **Non-bus burst parallel port for seamless, non-stop recording.**
- **Analog input comparator trigger**

Up to 10MHz Sampling



GENERAL DESCRIPTION

Offering very high system speed, the DVME-614 is a multichannel analog input board for VMEbus computers. Single channel full power input bandwidth is available up to 5MHz and may be sampled at up to 10MHz.

The analog input ranges of the A/D converter are selectable as unipolar 0 to +10V, or bipolar ±5V, or ±10V depending upon model. The gain on the DVME-614A may be user-selected 1x or 10x on two channels. The DVME-614E offers 16 single-ended or 8 differential inputs and programmable gain up to 100x.

Model DVME-614A uses a Simultaneous Sample/Hold (SSH) section. The SSH acquires signals on parallel channels at the same time, then the A/D converter rapidly digitizes each held signal sequentially. This provides phase correction and deskewing of multichannel correlated signals.

A/D data passes to an on-board First-In, First-Out (FIFO) data memory. The design can continuously collect analog data with non-stop converter triggering while data is simultaneously read from the FIFO. Functions such as FFT sampling cannot tolerate lost samples without increases in "arithmetic" noise during computation processing. The FIFO decouples the precise timing of the A/D section to conform with the block-oriented data transfers to the bus. Data may be transferred to mass storage peripherals such as disk or magnetic tape via the host computer bus interface under host software control.

The FIFO data output may also be routed under host software control to an on-board parallel digital data port. The parallel outport uses a universal ready/acknowledge transfer handshake adaptable to any remote parallel port. Typically, a FIFO half-full interrupt from the DVME-614 triggers an external processor to burst a fixed length block of samples.

The analog section of the DVME-614 is optimized for high signal quality and very low dynamic noise. The board is designed and qualified with low Total Harmonic Distortion

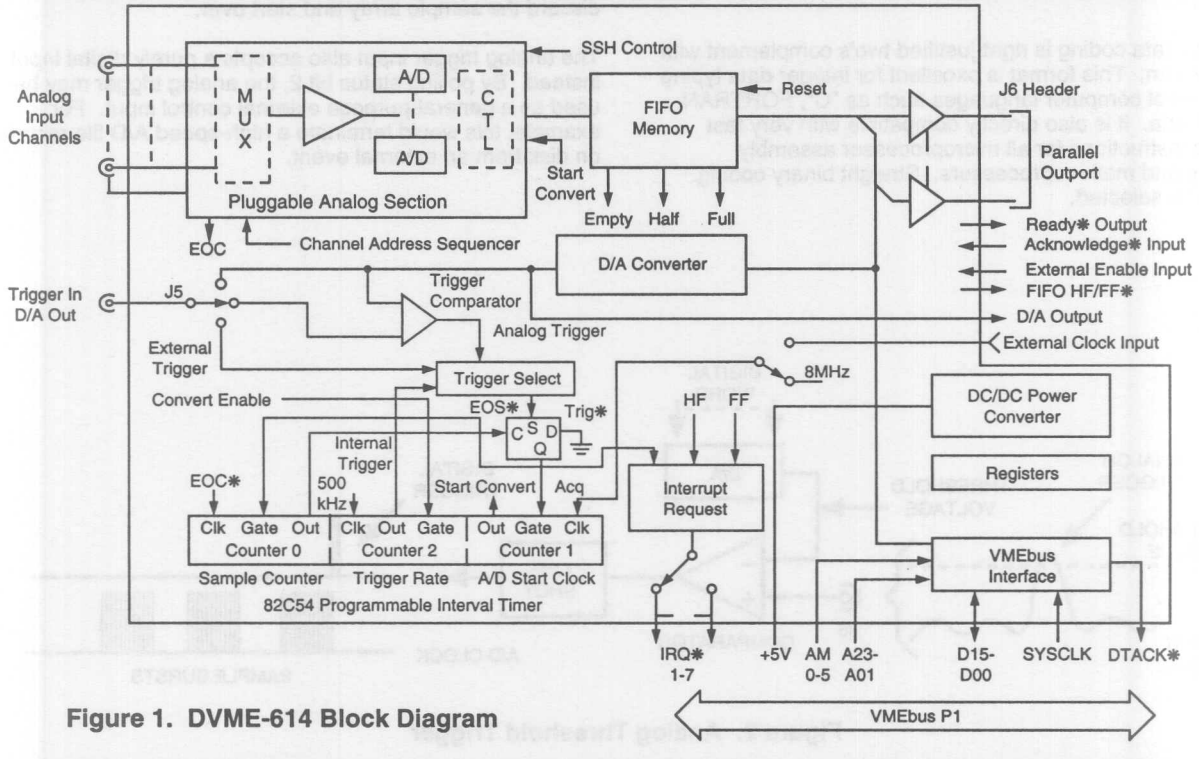


Figure 1. DVME-614 Block Diagram

(THD) characteristics. The DVME-614 is ideal as an FFT "front end" or DSP quantizer.

The A/D conversion timing section is designed for accurate multi-scan data acquisition. Software programmable timers control the interval between each conversion and each multichannel scan. A programmable sample counter allows sample blocks of specified length independent of FIFO length. The timer/counter section uses a precision on-board VMEbus clock and may be replaced by an external timebase. Timeout and sample count activities may be monitored from the computer bus using I/O status registers and/or programmable interrupts.

S/H-A/D triggering may use several sources under software control. The internal timebase is the normal trigger source although single conversions or scans may be directly commanded by host I/O register writes. An external trigger clock may also be used to precisely synchronize sampling with external events. This external trigger may start a single multichannel scan, or "N" multiple scans separated by programmable delays.

Analog sampling may also be level-triggered using an on-board analog comparator. The reference trigger level to the comparator is derived from an on-board 12-bit D/A converter. If preferred, the D/A converter may also be used as an analog output channel for any purpose.

The DVME-614 A-G have coaxial front panel signal connectors. Most connectors are for the sampled analog channels. The last connector is for a choice of the external timebase clock input, the external analog trigger level, or for the D/A output. The DVME-614E and J use a 25-pin connector. The computer interface for control and status uses 24-bit addressing. Board control and A/D data uses 16-bit VMEbus transfers. A single interrupt is generated for a variety of conditions under host software control. These include A/D data ready, sample count reached, FIFO half-full or FIFO full.

A/D output data coding is right-justified two's complement with sign extension. This format is excellent for integer data typing with high level computer languages such as "C", FORTRAN, Pascal or Ada. It is also directly compatible with very fast arithmetic instructions for all microprocessor assembly languages and math coprocessors. Straight binary coding may also be selected.

A high-efficiency, low-noise DC/DC converter provides quiet power to linear sections. The burst channel parallel port uses a 25-pin "D" front panel connector.

The DVME-614 is supplied with a set of low level device driver examples in assembly language and "C". These are supplied on universal MS-DOS disks. The drivers may be adapted to most host operating systems. The user manual has register and timing information for programmers to write their own software for any CPU or operating system. The drivers may operate in either interrupt or status mode.

High-Speed Dual-Channel Sampling

Model DVME-614F offers dual-channel simultaneous sampling using two 12-bit A/D converters triggered in parallel. Each converter may be sampled at a rate of up to 2MHz maximum. Data is interleaved into the FIFO memory with each start conversion pulse using swapped channel addressing (channel 0, channel 1, channel 0, . . .). Note that there will be twice as many samples in the FIFO versus the number of A/D start pulses. Model 614G is similar but uses two 14-bit 1MHz simultaneous A/D's.

Analog Trigger

The analog threshold trigger is ideal for monitoring noisy inputs such as a telemetry receiver or RF/IF channel. As soon as the trigger threshold is transitioned, the FIFO immediately starts filling with A/D samples. The raw comparator output may be polled from the VME bus in the status register, bit 2.

Since random noise may start this sampling process, the strategy is to collect a stream of A/D samples and quickly analyze if most of the samples contain valid data. If not, discard the sample array and start over.

The analog trigger input also accepts a purely digital input instead. By polling status bit 2, the analog trigger may be used as a general-purpose external control input. For example, this would terminate a high-speed A/D file recording on disk from an external event.

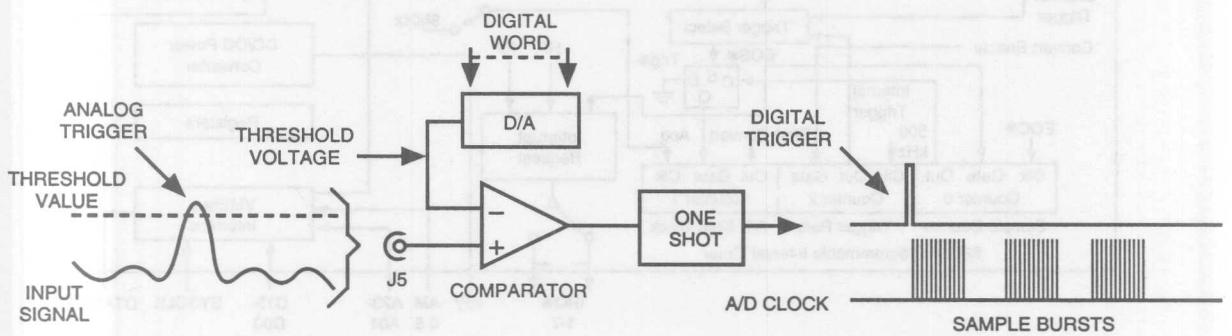


Figure 2. Analog Threshold Trigger

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FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	DVME-614A	DVME-614B	DVME-614C	DVME-614D	DVME-614E
Number of Channels	4 Simul.	4	4	1	16SE/8D
Input Configuration (non-isolated)	Single-Ended	Single-Ended	Single-Ended	Differential	SE or Diff.
Full Scale Input Ranges (user-selectable, gain = 1) [Footnote 1]	0 to +10V ±10V	0 to +10V ±10V ±5V	0 to +10V ±10V ±5V	±5V	0 to +10V ±10V ±5V
Input Bias Current	±1nA	±1nA	±1nA	±1nA	±1nA
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	2µs	2µs	2µs
Common Mode Voltage Range, maximum	—	—	—	±1V	±10V
Input Impedance [Footnote 9]	10MΩ	10MΩ	10MΩ	2kΩ	100MΩ
SAMPLE/HOLD					
Acquisition Time (FSR step, to 0.01% of FSR, max.)	900ns	750ns	200ns	50ns	750ns
Aperture Delay	15ns	20ns	20ns	10ns	20ns
Aperture Delay Uncertainty	±8ps	±100ps	±40ps	±7ps	±40ps
A/D CONVERTER					
Resolution	12 bits	14 bits	12 bits	12 bits	12 bits
Conversion Period	500ns	1.6µs	500ns	200ns	500ns
SYSTEM DC CHARACTERISTICS					
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1	±2	±1
Differential Non-linearity (LSB of FSR)	±0.75	±1	±0.75	±1	±0.75
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.1	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.3	±0.1
SYSTEM DYNAMIC PERFORMANCE [Footnote 3]					
Input Bandwidth (single channel, FSR input) [Footnote 10]	1MHz	200kHz	1MHz	2.5MHz	200kHz
Throughput to FIFO (single channel, gain = 1)	1.5MHz	500kHz	1.6MHz	5MHz [6]	2MHz
Throughput to FIFO (sequential channels, gain = 1) [Footnotes 4 & 2]	1MHz	330kHz	500kHz	—	500kHz
Total Harmonic Distortion [Footnote 3]	–72dB	–75dB	–72dB	–68dB	–72dB

ANALOG INPUTS	
Programmable Gains	See Footnote
Common Mode Rejection (DC - 60Hz)	–80dB (g = 100 for 614E)
Addressing Modes	1. Single channel 2. Simultaneous sampling 3. Sequential with autosequenced addressing 4. Random addressing by host software

A/D CONVERTER	
Output Coding	Positive-true right-justified straight bin. (unipolar) or right-justified 2's comp. (bipolar) with sign extension thru bit 15.
Trigger Sources (Software selectable)	1. Local Pacer frame clock 2. External TTL frame clock 3. Analog threshold comp.
A/D Sample Clock	1. Internal programmable 82C54 timer 2. Ext. TTL input, active high

FUNCTIONAL SPECIFICATIONS CONTINUED

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	DVME-614F	DVME-614G	DVME-614H	DVME-614J
Number of Channels	2 Simul.	2 Simul.	1	8 Simul.
Input Configuration (non-isolated)	Single-Ended	Single-Ended	Differential	Single-Ended
Full Scale Input Ranges (user-selectable, gain = 1) [Footnote 1]	0 to +10V ±5V	±5V 0 to +10V (special order)	±5V (other ranges special order)	0 to +2.5V ±5V, ±10V (separate unipolar & bipolar models)
Input Bias Current	±1nA	±1nA	—	±50nA (unipolar version)
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	1µs	—
Common Mode Voltage Range, maximum	—	—	±1V	—
Input Impedance [Footnote 9]	1kΩ	1MΩ	2kΩ	8kΩ (bipolar)
SAMPLE/HOLD				
Acquisition Time (FSR step, to 0.01% of FSR, max.)	165ns	350ns [14]	35ns	400ns
Aperture Delay	20ns	20ns	10ns	—
Aperture Delay Uncertainty	±40ps	±70ps	±3ps RMS	—
A/D CONVERTER				
Resolution	12 bits	14 bits	12 bits	12 bits
Conversion Period	400ns	500ns*	100ns [Footnote 15]	2µs (all chans. in simul. sampling)
SYSTEM DC CHARACTERISTICS				
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1.5	±1 max.
Differential Non-linearity (LSB of FSR)	±1	±1	±1	±1 max.
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 13]
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 13]
SYSTEM DYNAMIC PERFORMANCE				
Input Bandwidth (single channel, FSR input) [Footnote 10]	1MHz	500kHz	5MHz	100kHz
Throughput to FIFO (single channel, gain = 1)	2MHz	1MHz*	10MHz [15]	400kHz
Throughput to FIFO (sequential channels, gain = 1) [Footnotes 4 & 2]	4MHz (2 chans.)	2MHz (2 chans.)	—	250kHz/chan. (8 chans. simul.)
Total Harmonic Distortion [Footnote 3]	–70dB	–80dB	–65dB	–77dB

*Dual 2MHz 14-bit sampling is available on special order.

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A/D MEMORY	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024, 4096, or 16,384 A/D samples
TRIGGER CONTROL	
Programmable Interval Timer Type	82C54
Functions	1. A/D EOC sample count 2. A/D start rate (16-bit divisor) 4MHz max. on-board 3. Scan or frame rate 3 to
Pacer Sample Counter	65,536 samples. Drives the Acquire flag/interrupt gate for A/D start pulses.
82C54 Clock Source (user selectable)	1. Internal 8MHz crystal clock derived from VMEbus SYSCLK 2. External BNC TTL input, 10MHz max.
Scan Trigger Clock	125, 250, or 500kHz
Analog Trigger Input Range [Tech Note 5]	±10 Volts (not avail. on 614D)
Analog Trigger Response	2µs to set status flag
Analog Trigger Hysteresis	40mV
ANALOG OUTPUT	
Number of Channels	One channel
Function (user-selectable)	1. General purpose analog output 2. Threshold comparator for A/D trigger.
Resolution	12 bits
Output Voltage Range (user-selectable)	0 to +10V, ± 5V and ±10V at 5mA max.
Linearity	± 0.05% of FSR
Settling time (10V step)	5 microseconds to 0.05%
Input Coding	Straight binary
VMEbus INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Data Bus Width	16 bits using P1 connector.
Address Bus	24 address lines (A23-A01) plus 6 address modifiers.
Address Modifier Codes	39 hex or 3D hex, selectable.
VMEbus Interrupt	1 line, selectable IRQ 1-7*. Asserts maskable programmable 8-bit vector ID code.
Architecture	SAD24:SD16 slave consisting of 16 contiguous word registers.
Bus Interrupt Sources	Scan acquire flag (sample count), FIFO full or half full.
Control/Status Functions	FIFO reset, FIFO flags, interrupt select/status, trigger source, timer control/period, sample count load, parallel outport transfer status, A/D enable, MUX autosequence.
Data Transfer	Uses 16MHz VMEbus SYSCLK signal to generate DTACK* with selectable delay

PARALLEL DATA PORT	
Parallel Outport	16 lines, TTL levels from FIFO. Includes ready out, acknowledge in, and transfer enable in handshakes. Outport steering is software enabled.
Function	Asynchronous slave to remote master. Does not provide addressing. All data is sequential. The transfer enable input from a remote master is displayed as a status bit.
Parallel Port Loading	24mA out, 1.6mA in
Parallel Port Data Rate	4MHz max. to external processor
CONNECTORS	
VMEbus, P1	96-pin male DIN connector. The P2 connector is not used.
Analog Input Connectors	Four BNC bayonet coaxial, mounted on front panel. DB-25 used for 614E,J
Multipurpose Connector	5th BNC user-selectable for: a) Pacer trigger input b) Analog threshold comparator input c) D/A output
Parallel Port	Front panel 25-pin female DB-25S. Provides external clock in.
MISCELLANEOUS	
Power Required	+5V, ±5% at 3.0A max. from VMEbus.
Operating Temp. Range	0 to +60°C. Forced cooling is recommended.
Storage Temp. Range	–20 to +80°C
Relative Humidity	10% to 90%, non-condensing.
Altitude	0 to 10,000 feet.
Outline Dimensions	Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233,5 x 160 x 15,24 mm).
Weight	17 ounces (482 grams)
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Adjustments	Offset and gain per channel for SSH on DVME-614A. Offset and gain pots provided on DVME-614B,C,D,E,F,G.

Footnote:
Programmable gain is selectable on 2 channels on the DVME-614A only.

Note: 16MHz VMEbus SYSCLK is *required.*

FOOTNOTES

1. Resistor-programmed gain from X1 to X100 is available on DVME-614 E with increased settling delay at higher gains. Fixed gains of X1 and X10 on 2 channels, offering 1V ranges, are selectable on the DVME-614A.

2. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion, and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

3. THD test conditions are:
   1. Input freq. 500kHz (614A,F) 200kHz (614B,E)
      300kHz (614C) 1MHz (614D)
      100kHz (614G) 2MHz (614H)
   2. Generator/filter THD is -90dB minimum.
   3. THD computed by FFT to 5th harmonic.

      $$THD = 20 * \log 10 \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}$$

   4. Inputs are full scale –0.5dB. No channel advance.
   5. A/D trigger rate = 1.5MHz (614A), 500kHz (614B,C,E), 4MHz (614D), 2MHz (614F), 1MHz (614G), 10MHz (614H).

4. The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the DVME-614C were scanned, the maximum sample rate on any one channel would be 2µs X 4 channels = 8µs (125kHz per channel).

5. For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10V.

6. The input impedance of 10MΩ minimum avoids attenuation errors from external source resistance. For many applications, an in-line coaxial 50 Ohm shunt, inserted adjacent to the front connectors, is recommended to reduce reflections and standing wave errors.

7. Allow 20 minutes warmup time to rated specifications for models DVME-614B,G.

8. A 25-pin DB-25S connector is used for the DVME-614E,J.

9. Input impedance is shown with power on. Impedance with power off is 1500 Ohms or less.

10. Full power bandwidth is shown at approximately 3% distortion level. This is not the –3dB amplitude response which is at a higher but non-Nyquist frequency.

11. Avoid mixing external triggers which are a close submultiple of the internal A/D start clock to prevent lost samples.

12. The 5th SMA connector may be dedicated to either external trigger or external A/D clock.

13. DVME-614J bipolar input is user-selectable ±5V or ±10V per channel (default). Unipolar model is 0 to +2.5V. Total gain error over temperature range is ±4 LSB maximum. Total zero/offset error over temperature range is ±4 LSB maximum. Monotonicity: no missing codes over temperature range.

FIFO Data Format

A/D data is delivered as a stream from the FIFO memory. For multichannel inputs, this means that data is multiplexed. For example, for 4-channel inputs, the output channel sequence is 0, 1, 2, 3, 0, 1, ... Some applications may need this data de-multiplexed by software so that each channel's data is placed in its own separate buffer.

Simultaneous Sample/Hold

Four input signals are sampled at the same time using the DVME-614A's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired, they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors from conventional mux scanning. The DVME-614F, G, or J offers the same function at a higher speed using multiple simultaneous A/D's.

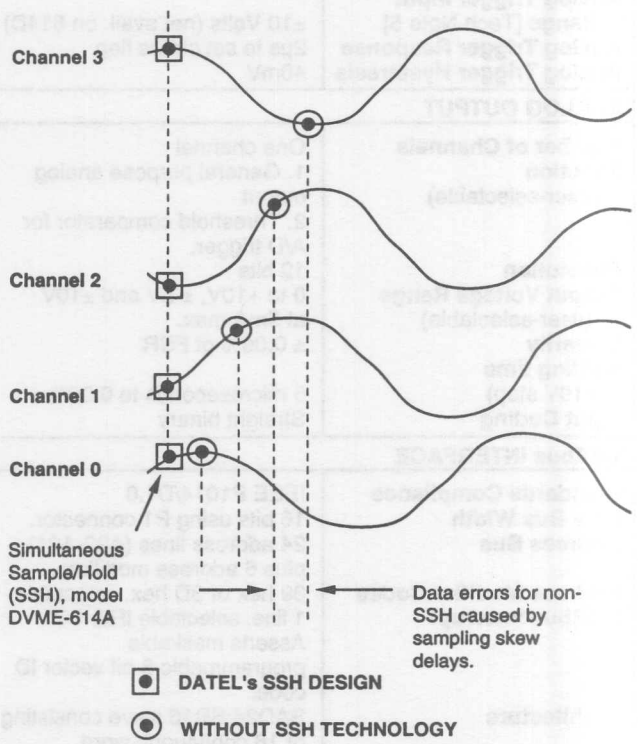


Figure 3. Advantage of DATEL's SSH Design

14. DVME-614G acquisition time is 350ns to ±0.003% of FSR.

15. Models DVME-614D,H use a single channel 12-bit A/D converter with ±5V inputs. An external A/D clock is required above 4MHz and the 82C54 timer must be bypassed. 10MHz sampling may continue until the FIFO memory is full.

Register Memory Mapping

The base address may be selected anywhere up to $FFFF00h on 32-byte boundaries.

Address (hex)	Direction	Description
BASE + 0	Write	Command Register
BASE + 0	Read	Status Register
BASE + 2	Write	Channel Address Register
BASE + 4	Write	D/A Data Register
BASE + 6	Write	FIFO Reset Register
BASE + 8	Not used	
BASE + 0Ah	Not used	
BASE + 0Ch	Read/Write	Interrupt Vector ID
BASE + 0Eh	Read	FIFO A/D Data Register
BASE + 10h	Read/Write	Counter #0 (82C54)
BASE + 12h	Read/Write	Counter #1 (82C54)
BASE + 14h	Read/Write	Counter #2 (82C54)
BASE + 16h	Read/Write	Control Register (82C54)

At power-up or VMEbus reset, all registers contain zeroes except the FIFO HF and FF bits. The registers may be programmed in any sequence as long as the command register is last. See user manual for full details.

Command Register (Write BASE + 0)

15-8	7 6 5	4	3	2	1 0
x-x	Interrupt Source FF HF ACQ	Port Bus*	Trig Pol	Cnvrt Enbl	Trigger Source

Status Register (Read BASE + 0)

15-8	7 6 5	4	3	2	1	0
x-x	FIFO Status FF HF EF	Ovr Smp Err	Xfr in Pro	Ana Trg Lvl	EOC Sts	ACQ Sts

Channel Address Register (Write BASE + 2)

15-8	7	6	5 4	3 2 1 0
x-x	Auto Incr	SSH Ctrl	Not Used	Channel Addr 3 2 1 0

D/A Data Register (Write BASE + 4)

15-12	11	10 -	- 1	0
x-x	DA1 MSB	DA2	DA11	DA12 LSB

FIFO Reset Register (Write BASE + 6)

15	00
x	x

Interrupt Vector Register (Read/Write BASE + 0Ch)

15-8	7	6	5	4	3	2	1	0
x-x	V7	V6	V5	V4	V3	V2	V1	V0

FIFO Data Register (Read BASE + 0Eh)

15	14	13	12	11	00
S	S	S	S	MSB	LSB

12-bit A/D data

15	14	13	00
S	S	MSB	LSB

14-bit A/D data

82C54 Counter Register
(Read/Write BASE + 10h - Counter #0)
(Read/Write BASE + 12h - Counter #1)
(Read/Write BASE + 14h - Counter #2)

15-8	7	6	5	4	3	2	1	0
x-x	C07	C06	C05	C04	C03	C02	C01	C00

Control Word Register (Read/Write BASE + 16h)

15-8	7	6	5	4	3	2	1	0
x-x	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

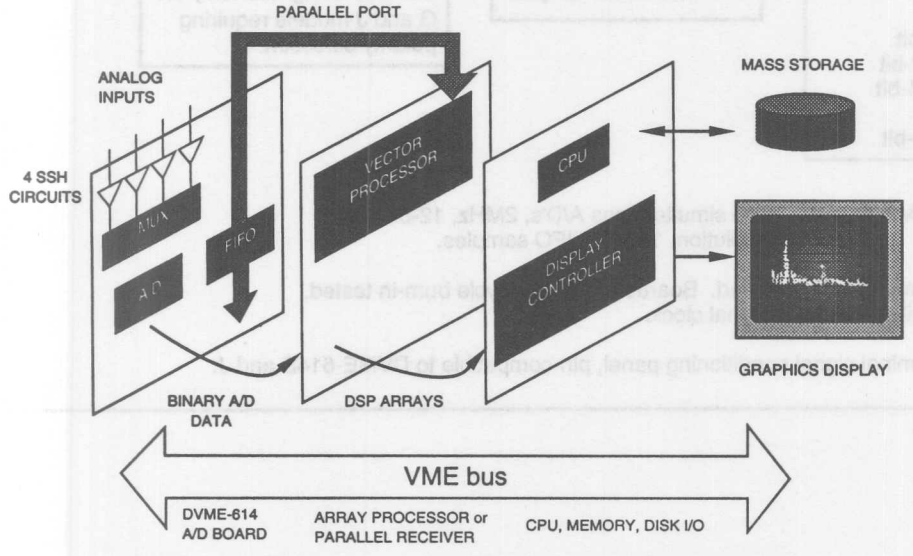


Figure 4. Array Pre-processing with the DVME-614

Array Preprocessing

Figure 4 shows the DVME-614 installed in a typical VME application. The DVME-614 may be connected to an array processor board via a parallel port or the VMEbus. The parallel port offers higher speed by offloading block data transfers from the VMEbus. A separate cable is required for the parallel port.

System Timing Diagram

Because of the flexibility of the local timing and trigger systems, the DVME-614 operates in many modes. Figure 5 shows multiple trigger configurations with the Acquire flag as an A/D converter clock gate. Triggering may be from internal or external clocks or from the analog comparator. For precise phase tracking, use both an external trigger and an external A/D start clock.

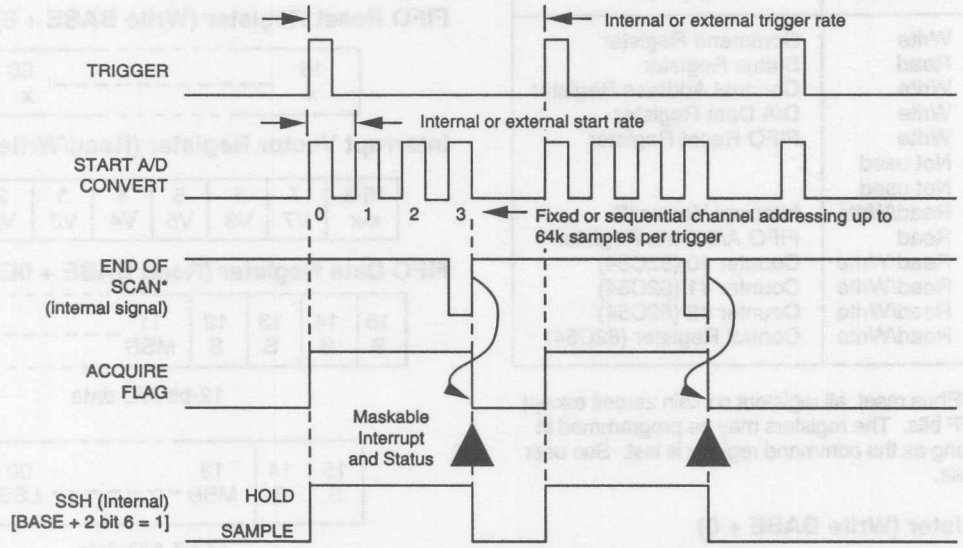


Figure 5. Trigger per Scan Mode

ORDERING INFORMATION

MODEL NUMBERING

DVME-614

A/D Type, Channels, Resolution	FIFO Memory Size	Input Range Polarity
A = 4 SE simul. chans., 12-bit B = 4 SE chans., 14-bit C = 4 SE chans., 12-bit D* = 1 D chan., 12-bit E = 16SE/8D chans., 12-bit F = 2SE simul. chans., 12-bit G = 2SE simul. chans., 14-bit H* = 1D chan., 12-bit J = 8SE simul. chans., 12-bit	1 = 1,024 A/D samples 2 = 4,096 A/D samples 3 = 16,384 A/D samples	A = Bipolar B = Unipolar Use this designator *only* for G and J models requiring polarity selection.

Example: DVME-614F3 Two simultaneous A/D's, 2MHz, 12-bit resolution, 16,384 FIFO samples.

A software disk and user manual are included. Boards are power-cycle burn-in tested.
*5 or 10MHz sampling available using external clock.

DVME-691 Screw terminal signal conditioning panel, pin-compatible to DVME-614E and J.

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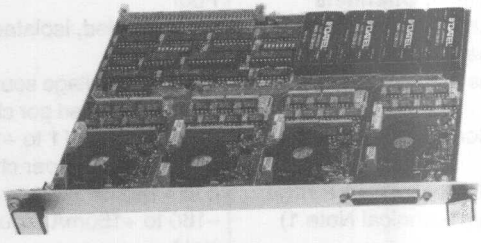
DATEL®
INNOVATION and EXCELLENCE

DVME-621

4-Channel, Isolated, Power Analog Output Board for VME Computers

FEATURES

- **4 isolated output channels**
- **Voltage mode or current loop**
- **Active mode 160mA loop output**
- **12-bit D/A resolution**
- **Selectable output ranges per channel**
- **For servos, controls, motors**
- **Industrial current loops**



GENERAL DESCRIPTION

Intended for industrial and medium-current test systems, DATEL's model DVME-621 is a four-channel power analog output board configured on a 6U VMEbus outline. Up to 100mA is available in voltage mode while current loops may be powered up to 160mA.

The DVME-621 is ideal for direct drive of servo amplifiers, small motors, deflection coils, actuators, power amplifiers, lamps, low power heaters and industrial controls. Other applications include robotics, power-supply testers, programmable amplifier loads and semiconductor screening systems.

Each output channel features dual isolation from adjacent channels and from the VMEbus. This offers freedom from ground loop problems and provides user safety and equipment protection. The 500V rms isolation is achieved with individual DC/DC power converters for each analog channel. Fast optoisolators buffer digital data and the channel logic is double buffered to eliminate data loading transients.

For maximum flexibility, each channel may be individually selected for current or voltage mode, unipolar or bipolar operations. The voltage output ranges are 0 to +11V or ±11V. Full scale current ranges are 0 to +160mA or ±160mA. Analog connections use a single front panel 25-pin connector. For accurate load voltage which is not affected by long power leads, all channels include sense inputs.

The DVME-621 appears as four VME memory locations in 24-bit standard address space. The board will accept 16-bit memory reference instructions in any computer language using any operating system. Data is stable within 11 microseconds after data write. User software may read back each channel to verify proper data loading and for board test. Very high speed memory loads may use DMA or block transfers from the host computer.

The DVME-621 uses one VME slot and has a 6U "double height" outline. All power is supplied from the +5V and +12V VMEbus power connections.

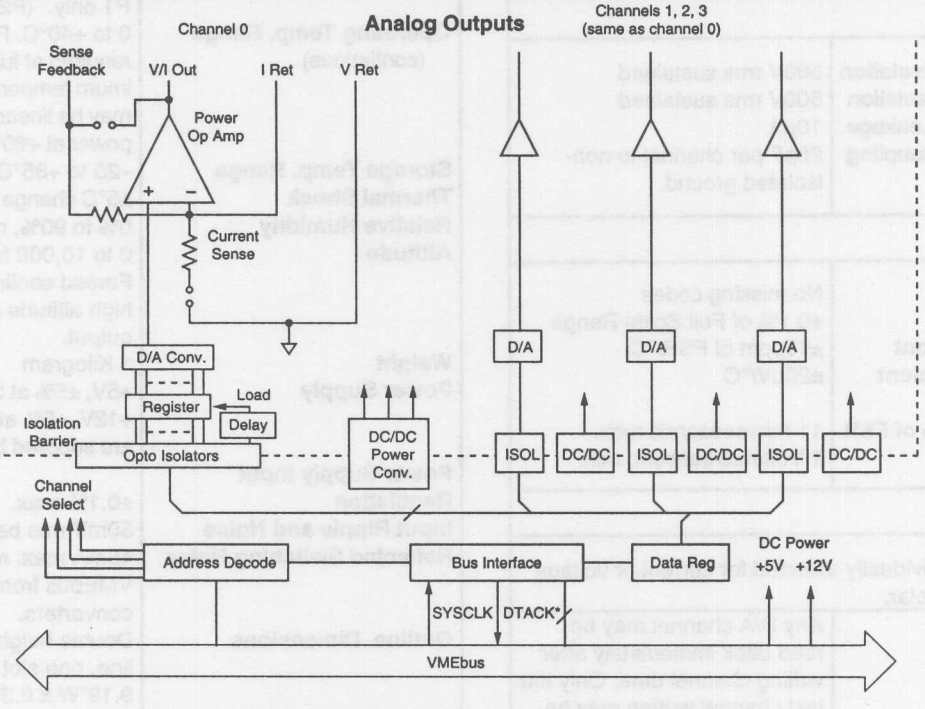


Figure 1. DVME-621 Simplified Block Diagram

SPECIFICATIONS
(Typical at +25°C unless noted)

ANALOG OUTPUTS	
Number of Channels	Four
Output Configuration (See Technical Note 3)	Single-ended, isolated per channel
Modes	Current or voltage source, individually selected per channel
Full Scale Voltage Range	0 to +11V or –11 to +11V at 0 to 100mA max. per channel.
Full Scale Current Range (See Technical Note 1)	0 to +160mA (source only) or –160 to +160mA (source or sink)
Current Mode Load	3 Ohms min. to 45 Ohms max. for full scale range.
Output Current Limit	±175mA max.
Output Impedance	500 milliohms max.
Output Protection	Short circuit recovery and open circuit voltage protection.
Overvoltage Protection	±14V max. (no damage). Reactive loads should externally clamp voltage spikes.
Stability	Stable for capacitive loads up to 0.1µF per channel
D/A Digital Inputs	Double buffered to prevent output transients during data transfers.
D/A Resolution	12 bits resolution, 1 part in 4096. (Bipolar configuration uses 11 data bits and one polarity bit).
Input Data Coding	Straight binary (unipolar) and offset binary (bipolar), right justified.

ISOLATION	
Channel-to-channel Isolation	500V rms sustained
Channel-to-VMEbus Isolation	500V rms sustained
Channel-to-channel Leakage	10µA
Isolation Capacitive Coupling	25pF per channel to non-isolated ground.

PERFORMANCE	
Monotonicity	No missing codes
Linearity Error	±0.1% of Full Scale Range
Zero Temp. Coefficient	±10ppm of FSR/°C
Offset Temp. Coefficient (after calibration)	±20µV/°C
Settling Time to 0.1% of FSR	11 microseconds max.
Slew Rate	1 Volt/microsecond min.

CONFIGURATION	
Channels may be individually selected for current or voltage mode, unipolar or bipolar.	
Data Readback	Any D/A channel may be read back immediately after writing channel data. Only the last channel written may be read back.
Feedback Control	Current and voltage sense feedback control is provided. Remote load sense is included for voltage mode.

VMEBUS INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Architecture	Memory mapped in four contiguous words in the bottom of a 256 location memory block. A24:D16 slave.
Memory Mapping	Decodes memory address lines A23 through A01 plus six address modifiers, AM5 - AM0.
Address Modifier Codes	39h or 3Dh, user selectable, "standard I/O" access. (Short I/O is also selectable).
Data Bus	16-bit transfer using VMEbus SYSCLK to generate DTACK* with selectable delay. Note: The 16MHz SYSCLK signal is required.
Interrupts	None

MISCELLANEOUS	
Analog Section Adjustments (See Technical Note 2)	Full scale and zero or offset multi-turn precision potentiometers are provided for each DAC channel. Recalibration is recommended every 90 days in stable conditions.
Analog Connector	One 25-pin DB-25S female mounted on front panel.
VMEbus Connector	96-pin DIN connector. Uses P1 only. (P2 is not installed).
Operating Temp. Range (continuous)	0 to +40°C. Forced cooling is required at full power and maximum temperature. Operation may be linearly derated to zero power at +60°C.
Storage Temp. Range	–25 to +85°C
Thermal Shock	±5°C change per minute max.
Relative Humidity	0% to 90%, non-condensing
Altitude	0 to 10,000 feet (0-3048m). Forced cooling is required at high altitude and full power output.
Weight	1 Kilogram
Power Supply	+5V, ±5% at 3.75A max. +12V, ±5% at 1.5A max. Both are supplied by VMEbus.
Power Supply Input Regulation	±0.1% max.
Input Ripple and Noise	50mV rms below 10MHz
Reflected Switching Noise	45mA max. reflected back to VMEbus from DC/DC converters.
Outline Dimensions	Double height 6U VME outline, one slot wide 9.19"W x 6.3"D x 0.6"H (233,5 x 160 x 15,24 mm)

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TECHNICAL NOTES

1. All current mode excitation is internally supplied via VMEbus. This is also referred to as "active" mode.
2. All DAC input registers are reset to zero or half scale (0800 hex) at power up or VMEbus reset depending on the unipolar/bipolar jumper selection. In either case, the output voltage is set at zero volts.
3. Since each output is isolated, they may be connected to either single-ended or differential receivers.

REGISTER MEMORY MAPPING

The memory base address may be selected anywhere using 24-bit addressing up to FFFF00h. 16-bit memory reference word instructions must be used. The registers may be programmed in any sequence and will accept host DMA or block transfer operations for highest speed. In readback mode, only the last register written will be returned. Read a DAC channel immediately after writing it to test each data load. In readback mode, bits 15-12 will always be logic "1".

Address (hex)	Direction	Description
Base + 0	Write	Load DAC0 data register
Base + 0	Read	Readback DAC0 data
Base + 2	Write	Load DAC1 data register
Base + 2	Read	Readback DAC1 data
Base + 4	Write	Load DAC2 data register
Base + 4	Read	Readback DAC2 data
Base + 6	Write	Load DAC3 data register
Base + 6	Read	Readback DAC3 data

DATA REGISTER FORMAT

15	14	13	12	11 - - - 0
x	x	x	x	MSB data LSB

On write, "x" bits 15-12 are "don't care". On readback, bits 15-12 will always be logic "1". In bipolar mode, the Most Significant Bit (MSB), bit 11, indicates polarity (0 = negative, 1 = positive).

MEMORY SIZING

Standard I/O addressing: Install E8 (standard)
Short I/O addressing: Install E7

OUTPUT POLARITY

Unipolar: Install E2
Bipolar: Install E1 (standard)

MEMORY BASE ADDRESS SELECTION

The 24-bit base address consists of three bytes. The top two most signficant bytes are decoded by two DIP switches, SW1 and SW2. Address bits 7 through 3 should be set to zero. Address bits 2 and 1 are decoded for the DAC data registers. The standard factory setting is FA0000 hex.

Upper byte:

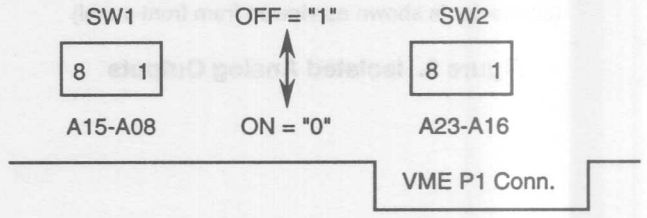
Address bit	A23	A22	A21	A20	A19	A18	A17	A16
DIP Switch SW2	8	7	6	5	4	3	2	1

Lower byte:

Address bit	A15	A14	A13	A12	A11	A10	A09	A08
DIP Switch SW1	8	7	6	5	4	3	2	1

Example: For a Base address of 10 0000h, turn off switch SW2-8 and leave all others on.

Switch location and orientation:



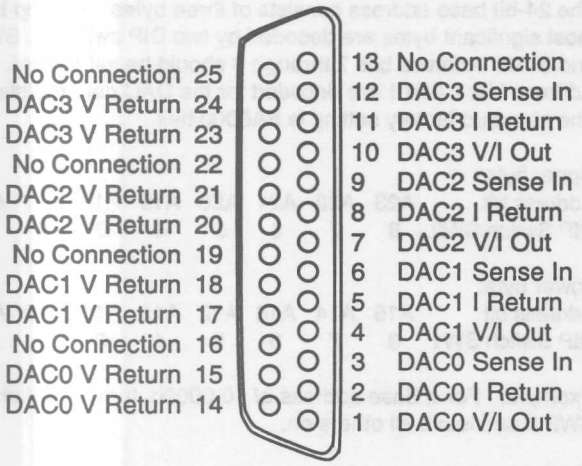
OUTPUT RANGE SELECTION

Important: Connect only the jumpers shown. Leave all other jumpers open.

Output Range*	DAC0	DAC1	DAC2	DAC3
±11V Bipolar	J3 2-3 J4 2-3 J2 2-3 J1 2-3 J5 1-2	J8 2-3 J9 2-3 J7 2-3 J6 2-3 J10 1-2	J13 2-3 J14 2-3 J12 2-3 J11 2-3 J15 1-2	J18 2-3 J19 2-3 J17 2-3 J16 2-3 J20 1-2
±160mA Current Loop Bipolar	J3 2-3 J4 2-3 J2 2-1 J1 2-1 J5 3-2	J8 2-3 J9 2-3 J7 2-1 J6 2-1 J10 3-2	J13 2-3 J14 2-3 J12 2-1 J11 2-1 J15 3-2	J18 2-3 J19 2-3 J17 2-1 J16 2-1 J20 3-2
0 to +11V Unipolar	J3 2-1 J4 2-1 J2 2-3 J1 2-3 J5 1-2	J8 2-1 J9 2-1 J7 2-3 J6 2-3 J10 1-2	J13 2-1 J14 2-1 J12 2-3 J11 2-3 J15 1-2	J18 2-1 J19 2-1 J17 2-3 J16 2-3 J20 1-2
0 to +160mA Current Loop Unipolar (source only)	J3 2-1 J4 2-1 J2 2-1 J1 2-1 J5 3-2	J8 2-1 J9 2-1 J7 2-1 J6 2-1 J10 3-2	J13 2-1 J14 2-1 J12 2-1 J11 2-1 J15 3-2	J18 2-1 J19 2-1 J17 2-1 J16 2-1 J20 3-2

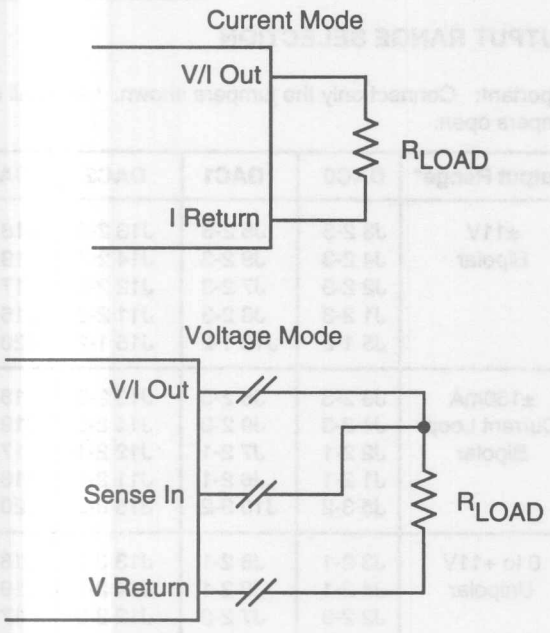
* ±10V and 0 to +10V ranges are available on each channel by removing J5, J10, J15, and J20 respectively. Alternate output ranges are available on special order.

ANALOG OUTPUT CONNECTOR (P2)



(connector is shown as viewed from front panel)

Figure 2. Isolated Analog Outputs



Important: Connect sense at the load.

Figure 3. Output Connections

PROGRAMMING EXAMPLE

The DVME-621 requires simple memory reference instructions in any language. 16-bit word operations should be used. Certain systems may require modification using a function which allows accesses to real physical memory from virtual memory. The following example in the "C" language loads the data channels:

```
/* 28jan93 ldc */
#include <stdio.h>
#define BASE 0xFA0000 /* change this for your system !! */

main( ){
/* set up pointers to data registers. basptr is the base address
of the board. */

unsigned short   *basptr,   /* BASE address */
                 *chan0,    /* DAC channel 0 */
                 *chan1,    /* DAC channel 1 */
                 *chan2,    /* DAC channel 2 */
                 *chan3;    /* DAC channel 3 */

/* Initialize pointers */

  basptr = ( unsigned short *) BASE;
  chan0 = basptr + 0;
  chan1 = basptr + 2;
  chan2 = basptr + 4;
  chan3 = basptr + 6;

/* Now load -full scale, half scale, +1 count and +full scale
values into 4 channels. */

  *chan0 = 0x0000;   /* -FS */
  *chan1 = 0x0800;   /* half scale */
  *chan2 = 0x0801;   /* +1 LSB */
  *chan3 = 0x0FFF;   /* +FS -1 LSB */

} / * end of program */
```

ADDRESS MODIFIER SELECTION

Address Modifier	Function	Jumper
2D hex	Short I/O supervisory access	E9
29h or 2Dh	Short I/O non-privileged or supervisor access	E10
3D hex	Standard I/O supervisor access	E11
39h or 3Dh	Standard I/O non-privileged or supervisor access	E12

ORDERING INFORMATION

MODEL	DESCRIPTION
DVME-621	4-channel, VMEbus, power output analog board.
DVME-691D	19" rack mount screw terminal adapter and cabling

Alternate output ranges are available on special order.

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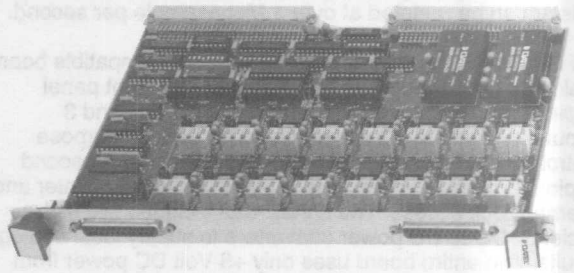
DATEL®
INNOVATION and EXCELLENCE

DVME-622

8/16-Channel, Fast Simultaneous VME bus Analog Output Board

FEATURES

- **8 or 16 analog outputs**
- **12-bit D/A resolution**
- **3 microsecond settling time**
- **Simultaneous update**
- **Trigger timer interrupt**
- **Digital I/O (4-in, 3-out)**
- **Output ranges selectable per channel**



DESCRIPTION

Many applications require phase-synchronous analog outputs. Examples include precision system simulation and coherent field generation in process control, audio, acoustics and sonar. The DVME-622 is a high density analog output board with up to 16 signal channels. Each Digital to Analog Converter (DAC) channel may be individually selected for full scale output ranges of 0 to +5V, 0 to +10V, ±5V, ±10V, or ±2.5V. All outputs are buffered and will deliver ±0.025% accuracy from 0 to 5 milliamps output load. The DVME-622 is installed in a host VMEbus computer.

To achieve the simultaneous update capability, each channel input register is double buffered. The registers are successively loaded by the host computer then all channels are updated by host command or trigger. If preferred, each channel may also be operated in the non-concurrent transparent mode under program control with random addressing or single channel operation.

For applications requiring a precision clock to sequence the output waveforms, the DVME-622 includes a software-programmable trigger. The trigger strobes the simultaneous update and posts a status bit or interrupt to the host computer. Upon detecting the trigger, the host may block-load the next data frame. The trigger may be derived from an internal crystal-stabilized timer or from an external timebase. The external trigger and external clock options make the DVME-622 fully synchronous with external events. The timing section also includes a spare counter, usable for any purpose.

For repeating frame scan applications, the DVME-622 includes an autoincrement mode. In this mode, memory block transfer instructions will automatically load up to 16 channels at very high speed from a buffer in the host. The DVME-622 will digitally steer each analog data word to successive DAC input registers while using the same memory data register address. The user's program simply maintains a CPU register as a downcounter to terminate each block transfer. Typically, the trigger and autoincrement modes are used together where the host loads the next block after detecting the trigger status signal from the last simultaneous update.

The combination of a precision frame clock trigger, autoincrement channel addressing and high speed simultaneous block loading make the DVME-622 ideal for artificial waveform applications. Such waveform generators continuously loop through a large RAM buffer containing a synthetic composite digitized analog signal.

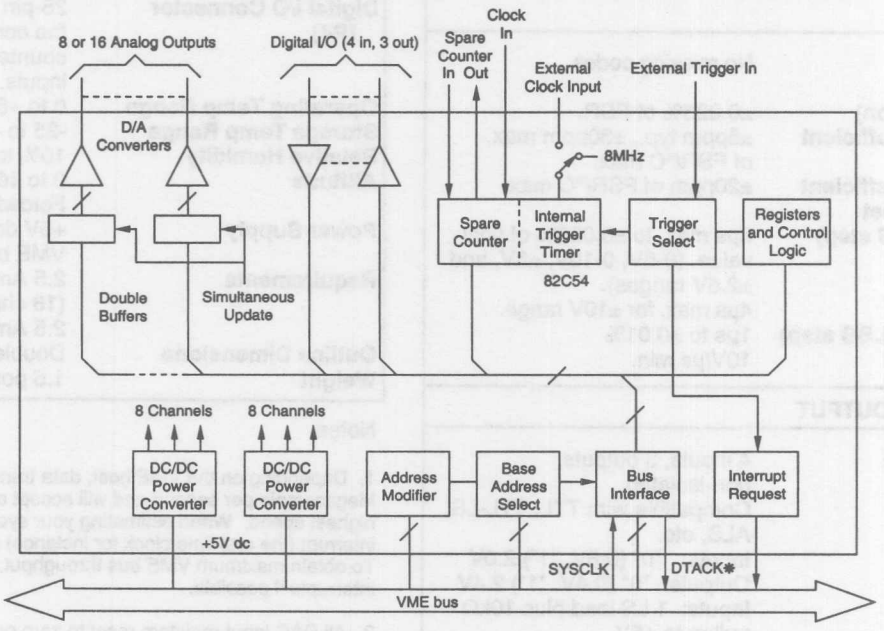


Figure 1. DVME-622 Block Diagram

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Fast settling rates are another feature of the DVME-622. Full scale step response of each DAC channel is 3 microseconds. Block transfers of input data may occur faster than individual DAC channel analog settling times. Each DAC channel input register can be updated at over 1 Megasample per second.

The DVME-622 is configured on a 6U VME compatible board. Analog signal connections are made using a front panel 25-pin "D" connector. Seven channels (4 inputs and 3 outputs) of discrete I/O are provided for general purpose control and monitoring of external logic devices. A second 25-pin "D" connector provides digital I/Os, spare counter and external clock access. The DVME-622 includes two high efficiency DC to DC power converters to supply local analog circuits. The entire board uses only +5 Volt DC power from the VME bus. The board is compatible with all popular computer languages although the highest speed will require assembly language. A comprehensive user's manual is included with the board as well as a MS-DOS diskette containing example source programs.

SPECIFICATIONS

(typical at +25°C, dynamic conditions, unless noted)

ANALOG OUTPUTS

Number of Channels	8 or 16
Output Configuration	Single-ended, non-isolated
Full Scale Output Ranges	0 to +5V, 0 to +10V, ±5V, ±10V, and ±2.5V, individually selectable per channel.
Output Current	±5mA min. (source or sink), short-circuit protected to ground.
Resolution	12 binary bits.
Input Data Coding	Straight or offset binary, positive true coding. Data is right justified.
Output Impedance	50 milliohms
Channel Addressing Modes	Random, simultaneous or auto-increment sequential.

PERFORMANCE

Monotonicity	No missing codes
Linearity Error (after calibration)	±0.025% of FSR.
Temperature Coefficient of Gain	±5ppm typ., ±30ppm max. of FSR/°C max.
Temperature Coefficient of Zero or Offset	±20ppm of FSR/°C max.
Settling Time (FS step)	3µs max. to ±0.025% of final value. (0-5V, 0-10V, ±5V, and ±2.5V ranges). 4µs max. for ±10V range.
Settling Time (1 LSB step)	1µs to ±0.01%
Slew Rate	10V/µs min.

DIGITAL INPUT/OUTPUT

Number of Lines	4 inputs, 3 outputs, non-isolated
Logic Levels	Compatible with TTL, TTL-LS, ALS, etc. Inputs: "0" (0.8V, "1") 2.0V Outputs: "0" (0.4V, "1") 2.4V
I/O Loading	Inputs: 1 LS load plus 10kΩ pullup to +5V. Outputs: 24mA source or sink

COUNTER/TIMER

Function	Used as an update strobe for each multichannel DAC frame
Frequency Range	2MHz to 536.87 Sec (32-stage binary or BCD divider). Use external clock to increase range.
Frequency Stability	±50ppm/°C.
Spare Counter	16-stage binary divider usable for any purpose. Will divide input signals from 2 to 65,535. Includes counter input, output, and clock, 1 TTL-LS load, 10MHz max. clock input.

VME BUS INTERFACE

Standards Compliance	IEEE P1014/D1.0
Architecture	Memory mapped in 8 contiguous word locations on 256-byte boundaries. A24:D16 slave.
Memory Mapping	Decodes memory address lines A23 through A08 plus six address modifiers, AM5-AM0.
Address Modifier Codes	39h or 3Dh, selectable
Data Bus	16-bit transfer using VME bus SYSCLK signal to generate DTACK* with selectable delay. (Note: SYSCLK is required)
Trigger Interrupt	1 interrupt, selectable on IRQ 1-7 plus maskable programmable 8-bit vector ID.

MISCELLANEOUS

Analog Section Adjustments (every 90 days)	Full scale gain and zero or offset potentiometers are provided for each DAC channel. See note 2.
Analog Connector [P3]	25-pin DB-25S female, incl. the external trigger input.
Digital I/O Connector [P4]	25-pin DB-25S female, incl. the connections to spare counter and external clock inputs.
Operating Temp Range	0 to +60°C
Storage Temp Range	-25 to +85°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 ft (0-3048 m). Forced cooling recommended.
Power Supply Requirements	+5V dc, ±5% supplied from VME bus. 2.5 Amps typ., 4.0 Amps max. (16 channels), 1.5 Amps typ., 2.5 Amps max. (8 channels).
Outline Dimensions	Double height 6U VME outline.
Weight	1.5 pounds (0.7kg)

Notes

1. Depending on the VME host, data transfers may occur at over 1 Megasample per second and will accept a host DMA controller for highest speed. When estimating your system timing, account for any interrupt (the real time clock for instance) and DRAM refresh delays. To obtain maximum VME bus throughput, disable all host system interrupts if possible.

2. All DAC input registers reset to zero or to half scale (0800 hex) on power-up or reset depending on the unipolar/bipolar switch selection. In either case, the output voltage level is set to 0 Volts.

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I/O REGISTER MAPPING

The memory base address may be selected anywhere using 24-bit addressing up to FFFF00h on 256-byte boundaries. At power-up or VME bus reset, all control registers contain zeroes. The DAC data register should be programmed after setting up the channel address and command mode. The 82C54 registers must be programmed in a specific sequence - discussed in the User Manual. 16-bit memory reference word instructions must be used. Do not use read-modify-write or test-and-set instructions at locations with separate co-located read and write registers. Unlisted registers are not used.

Address (hex)	Direction	Description
BASE + 0	Write	Command and Vector Register
BASE + 0	Read	Status Register
BASE + 2	Write	DAC Channel Address Register
BASE + 2	Read	Interrupt Vector Register
BASE + 4	Write	DAC Data Register
BASE + 6	Write	Simultaneous Update Register
BASE + 8	Read/Write	Counter 0 (82C54)
BASE + 0Ah	Read/Write	Counter 1 (82C54)
BASE + 0Ch	Read/Write	Counter 2 (82C54)
BASE + 0Eh	Read/Write	Control Word Register (82C54)

"x" bits are "don't care"

Command and Vector ID Register (Write BASE + 0)

15 — 8	7	6	5	4	3	2 1 0
Interrupt Vector Identification	Siml Updt Sel	Siml Updt Mode	Ext/ Int Trig	Chan Auto Incr	I N T	Digital Outport 2 1 0

Digital Outport [Bits 2, 1, 0] — Discrete digital outputs are written to these bits.

Trigger Interrupt Enable [Bit 3] — 0 = Disable interrupts; 1 = Enable interrupts

The trigger will cause an optional VME bus interrupt using bit 3.

Channel Address Autoincrement [Bit 4] — 0 = No channel increment; 1 = Increment channel address after a DAC data register write.

In the non-increment mode (bit 4 = 0), successive writes to the DAC data register will load into a single DAC channel selected by the last address written into the channel address register.

In autoincrement mode (bit 4 = 1), the channel address will advance after each data register write. The address will cycle around to channel 0 after reaching channel 15, modulo 16.

Trigger Source Select [Bit 5] — 0 = Internal trigger; 1 = External trigger

The trigger may be supplied either from the internal clock (counters 0 and 1) or from an external digital trigger input. In simultaneous update mode (bit 6 = 1, bit 7 = 1), the trigger strobes all DAC channels simultaneously from previously written DAC data.

Simultaneous Update Mode [Bit 6] — 0 = Update via the simultaneous update register (Write BASE + 6). 1 = Update via internal or external trigger.

Simultaneous update causes all 8 or 16 DAC channels to be loaded with data that was last written to their input registers. If command bit 6 = 0, the trigger will be inhibited.

Simultaneous Update Select [Bit 7] — 0 = Transparent mode (immediate DAC conversion of input data) 1 = Hold data until update.

With bit 7 = 0, DAC analog outputs will follow their input data values as fast as those values are written. If bit 7 = 1, updating the DAC outputs will wait until the trigger or a write to the update register.

Interrupt Vector ID [Bits 15 through 8] — The actual interrupt service routine must be loaded at ID x 4 + Vector Base Register.

Status Register (Read BASE + 0)

15	14	13	12	11 – 8
Update Ready Status	Over Run Error	Not Used X	Interrupt Enable Status	Current Channel Address 3 2 1 0

7	6	5	4	3 2 1 0
Simul. Update Select	Simul. Update Mode	External/ Internal Trigger	Chan Addrs Auto Increment	Digital Inport 3 2 1 0

Bits 4-11 may be used to verify bits loaded into the command register.

"X" bits are not used and should be ignored.

Digital Inport [Bits 3, 2, 1, 0] — Discrete digital inputs may be read in these bits.

Status Bits [Bits 7-4] — These bits follow the corresponding bits in the command register.

Current Channel Address [Bits 11-8] — These bits indicate either the last address written into the channel address register or the next channel address to be written to by the next DAC data write. These addresses will sequence from channel 0 to 15, modulo 16 in autoincrement mode.

Interrupt Enable Status [Bit 12] — 0 = Interrupts disabled 1 = Interrupts enabled

Bit 13 — Not used.

Over Run Error [Bit 14] — In trigger update mode (command 6 = 1), this bit will be set to one if a trigger occurs before the next load of the DAC data register. Any write to the command register resets bit 14 to zero.

Update Ready Status [Bit 15] — With command bit 7 = 1, a write to the simultaneous update register will set bit 15 to one. The trigger will reset this bit to 0, indicating that the next frame of data may be loaded. If a trigger occurs before bit 15 is set to 1, the over run error bit will be set to 1.

Bit 15 is normally polled to detect the trigger after loading the data registers. Bit 15 will stay at zero if command bit 6 = 0.

Channel Address Register (Write BASE + 2)

15 - 4	3 2 1 0
Not Used	Channel Address 3 2 1 0

In non-autoincrement mode, these bits select the address of the next channel to be written to by the DAC data register.

In autoincrement mode, these bits determine the starting channel address. After each data register load, addressing is automatically sequenced. The addressing cycles around to channel 0 after reaching channel 15.

Interrupt Vector ID Register (Read BASE + 2)

15 - 8	7 - 0
Not Used	Vector ID

This register may be used to verify the vector ID code written into bits 15 through 8 of the COMMAND Register.

DAC Data Register (Write BASE + 4)

15 - 12	11 - 0
Not Used	DAC MSB DAC LSB

12-bit DAC data are right justified with the most significant bit at bit 11. In bipolar coding, bit 11 indicates polarity (0 = negative, 1 = positive).

Simultaneous Update Register (Write BASE + 6)

15 - 8	7 - 0
Not Used	x - x

This register has two separate functions. If command bit 6 = 0 and command bit 7 = 1, the analog outputs of all DAC channels will be updated at the same time by writing any value to this register. If command bit 6 = 1, writing any value to this register will set the trigger ready status flag (status bit 15) to 1. The flag will remain set until cleared to zero by the trigger. This sequence provides a handshaking to load data frames without losing samples.

ORDERING GUIDE

Model	Number of channels
DVME-622A	8
DVME-622B	16
DVME-622SRC	Setup/Config. source disk, MS-DOS compatible

Boards are fully tested, calibrated, and supplied with a user manual. The setup and configuration program is on an MS-DOS diskette. All boards are burn-in tested under power-cycled conditions and include a one year warranty

DVME-691A Screw terminal panel for 19-inch rack mount. Includes flat cables to DVME-622.

82C54 Programmable Interval Timer

[Refer to the DVME-622 User Manual for detailed programming information]

Counter Register (Read/Write BASE + 8 - Counter #0)
(Read/Write BASE + 0Ah - Counter #1)
(Read/Write BASE + 0Ch - Counter #2)

15 - 8	7	6	5	4	3	2	1	0
x - x	C07	C06	C05	C04	C03	C02	C01	C00

Control Word Register (Read/Write BASE + 0Eh)

15 8	7	6	5	4	3	2	1	0
x - x	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Select Counter

SC1	SC0	
0	0	Select counter #0
0	1	Select counter #1
1	0	Select counter #2
1	1	Read back command

Read/Load

RL1	RL0	
0	0	Counter latch operation
0	1	Read/Load LSB only
1	0	Read/Load MSB only
1	1	Read/Load LSB then MSB

Mode

M2	M1	M0	
x	1	0	Rate generator
1	0	0	Software trigger
1	0	1	Hardware trigger

BCD

BCD	
0	16-bit binary count
1	4-decade binary coded decimal count

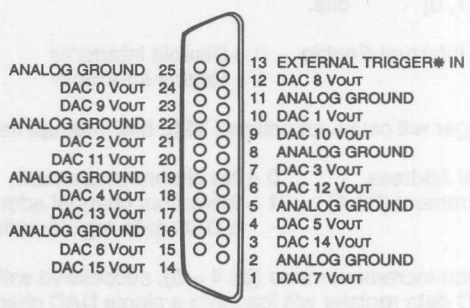


Figure 2. Analog Output Channel Connector - P3

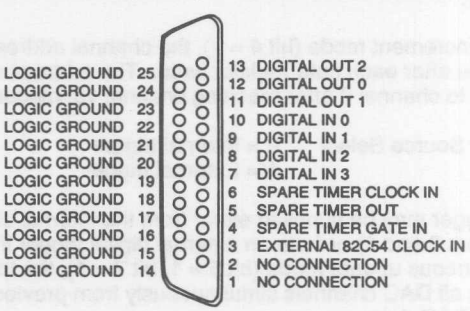


Figure 3. Digital I/O Connector - P4

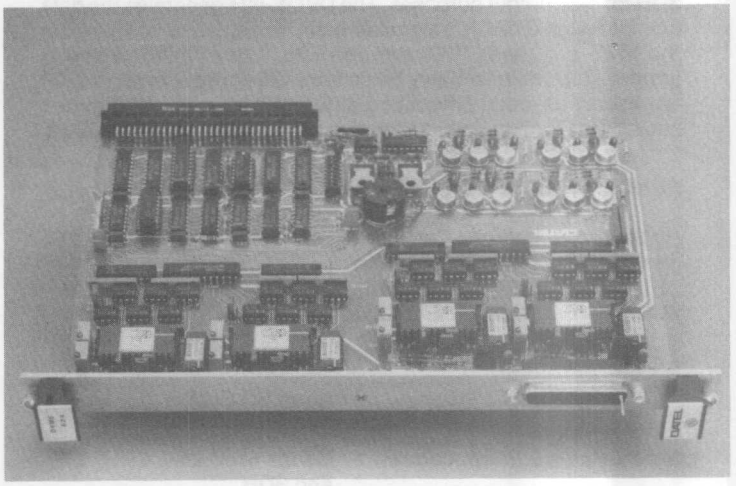
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DVME-624
Isolated, 4-Channel 12-Bit, VMEbus D/A Board

FEATURES

- 4-Channel memory mapped D/A board
- 300 VRMS channel-to-channel and channel-to-bus isolation
- Hardware compatible with VMEbus specifications
- On-board isolated dc-to-dc power converter
- Optional 6 μS or 30 μS settling time models
- 12-Bit resolution
- Choice of output voltages:
  a. 0 to 5V dc
  b. 0 to 10V dc
  c. ±2.5V dc
  d. ±5V dc
  e. ±10V dc
- Optional 4-to-20mA current loop capability conforming to ISA standards
- ±1/2 LSB differential non-linearity
- ±0.05% Full-scale range accuracy



GENERAL DESCRIPTION

The DVME-624 is DATEL's 12-bit, 4-channel D/A board, totally compatible with VMEbus specifications. In a typical application the board provides analog outputs in real-time to the host system at a high speed. The different full-scale output voltage ranges the board offers conform to process control and test and measurement industrial requirements.

Each channel is configurable to different output voltage ranges. The salient feature of the DVME-624 board is the 300 VRMS channel-to-channel and channel-to-bus isolation. The board uses high performance optoisolators to provide the isolation. An on-board dc-to-dc power converter provides isolated power to each D/A converter section.

The isolation makes the DVME-624 an ideal choice for applications where a low-level signal superimposes a high voltage such as in testing of power supplies. The channel-to-bus isolation protects the host system against any catastrophic damages due to an external malfunction such as an actuator failure.

The DVME-624 offers ±1/2 LSB differential non-linearity and operates at ±0.05% full-scale range accuracy. The DVME-624 models are available at two different settling times. The lower cost DVME-624C1 and DVME-624V1 models offer 30 μS settling time and the DVME-624C2 and DVME-624V2 models offer 6 μS settling time. The DVME-624 may be obtained with an optional 4-to-20mA industrial current loop output in addition to the voltage outputs. Refer to the ordering information for models with current loop option.

Functionally, the digital data from the VME host system is transferred through a 12-bit data register to one-of-four D/A sections. The DVME-624 converts the 12 most significant bits from the VME data bus to an analog output. Data from the host system may be in straight binary, offset binary, or 2's complement coding. The D/A converter sections are optically isolated from the VME interface logic. The DVME-624 uses monolithic D/A converters to increase the product's reliability and endurance.

The DVME-624 D/A boards will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the DVME-624. The DVME-624 is shipped with an 680X0 assembly language diagnostic program example on an MS-DOS formatted diskette.

ORDERING INFORMATION

DVME-624

- 1 — 30 μS Settling time
- 2 — 6 μS Settling time
- V — Voltage output only
- C — Voltage and 4-to-20 mA current loop output

Each board includes a user manual.

VME Interface

The DVME-624 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to the address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-624 generates the data acknowledge (DTACK*) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK* signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems. Figure 1 shows the functional block diagram of the DVME-624 D/A board.

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, V_{exc} = +24V dc, R_{loop} = 250 ohms, unless otherwise specified.)

INTERFACE SPECIFICATIONS

Data Bus	16 bits
Address Bus	Short I/O Space, 16 address lines
Address modifiers codes	Codes used 29H, 2DH, 39H, and 3DH
Memory Mapping	Short I/O space, user or supervisor 256 bytes allocated per board (A16:D16 slave).

INTERNAL HARDWARE REGISTER/SOFTWARE ASSIGNMENTS

Register Memory Mapping

Relative Address	Function	READ/WRITE
0 through 63	Board Identification Code	Read Only
64 through 127	See Note 1	Read Only
128 through 159	See Note 2	Write Only
160	D/A Channel 0	Write Only
162	D/A Channel 1	Write Only
164	D/A Channel 2	Write Only
166	D/A Channel 3	Write Only
168 through 255	See Note 2	Write Only

Note 1: These addresses are redundant with ID PROM addresses, base + 0 through base + 63.

Note 2: These addresses are redundant in 8-byte blocks with the DAC data registers, base + 160 through base + 166.

The VMEbus SYSCLK signal is required.

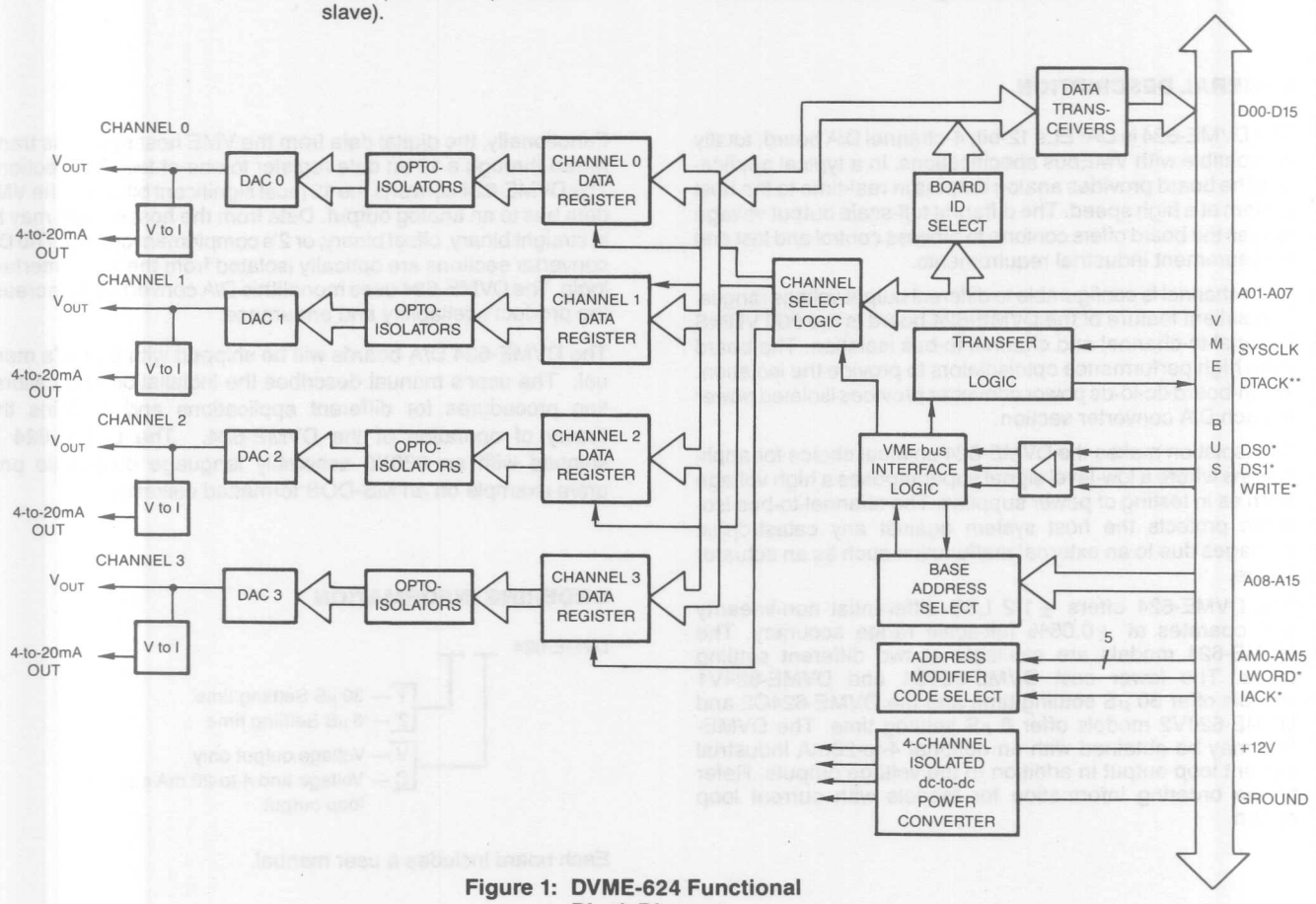


Figure 1: DVME-624 Functional Block Diagram

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CONNECTOR SPECIFICATIONS

VME bus — P1 . . . . . 96-pin male DIN connector

Analog Output — J1 . . . . . 25-pin D Type female connector, Amp P/N 745783-1 or equivalent

ANALOG OUTPUT SPECIFICATONS

Number of Channels 4

Channel-to-channel Isolation . . . . . 300 VRMS, sustained maximum

Output full-scale voltage ranges (Selectable per channel) . . . . . 0 to 5V dc
0 to 10V dc
±2.5V dc
±5V dc
±10V dc (standard)

Input data coding . . . . . Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary

Resolution . . . . . 12 Bits. Uses 12 most significant data bits from the data bus. Ignores bits D0 through D3.

Reset . . . . . Minus full-scale, output resets to 0.000V dc

Current Loop . . . . . 4-to-20 mA. Meets ISA standard 550.1 Type 4 Class U

Excitation Voltage (User-supplied) . . . . . 15 to 36V dc

PERFORMANCE

Specification	Minimum	Typical	Maximum
Accuracy	0.05% of FSR	—	—
Differential non-linearity	—	—	0.5 LSB
Zero temperature drift	—	3 ppm/°C	5 ppm/°C
Offset temperature	—	5 ppm/°C	10 ppm/°C
Gain temp drift	—	15 ppm/°C	30 ppm/°C
Settling time:			
DVME-624V1 DVME-624C1	—	30 μseconds	—
DVME-624V2 DVME-624C2	—	6 μseconds	—
Output current	—	±5 mA	—
Output impedance	—	50 milliohms	—

Note: The 6 microsecond option should be selected for low transient applications such as amplifier inputs.

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1.0A typical, 1.2A maximum
+12V dc ±2.0% at 0.4A typical, .7A maximum

CURRENT LOOP

Specification	Minimum	Maximum
Accuracy	0.1% of FSR	—
Excitation (user-supplied)	15V dc	36V dc
Load resistance	100 Ohms	1000 Ohms
Isolation channel-to-channel	300 VRMS	—
Isolation output-to-bus	300 VRMS	—

PHYSICAL CHARACTERISTICS

Outline Dimensions . . . . . 9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)

Weight . . . . . 9.6 oz (272.3 grams)

Operating temperature range . . . . . 0 to 60°C

Storage temperature range . . . . . −20 to +80°C

Relative humidity . . . . . 0 to 90%, non-condensing

DVME-624 ANALOG OUTPUT CONNECTOR J1

The DVME-624 provides analog outputs using the J1 connector. Depending on the model, the J1 connector contains voltage and current loop outputs. Figure 2 shows the output signals on the J1 connector.

PIN NUMBER	DESCRIPTION
1	DAC 0 V OUT
2	DAC 0 I LOOP
3	DAC 0 V LOOP
4	DAC 1 V OUT
5	DAC 1 I LOOP
6	DAC 1 V LOOP
7	DAC 2 V OUT
8	DAC 2 I LOOP
9	DAC 2 V LOOP
10	DAC 3 V OUT
11	DAC 3 I LOOP
12	DAC 3 V LOOP
13	
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	

Figure 2: Analog output pinout details

DVME-624 DATA FORMAT

The DVME-624 uses a 12-bit D/A converter for converting the digital data to analog signal. The board uses the 12 most significant bits of the VME data lines as input signals. Figure 3 shows the data format the DVME-624 is designed for.

15		4	3	2	1	0
MSB	DATA BITS	LSB	X	X	X	X
			Not Used by DVME-624			

Figure 3: DVME-624 data format

DVME-624 Board Identification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	2	
+ 1F	4	

DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

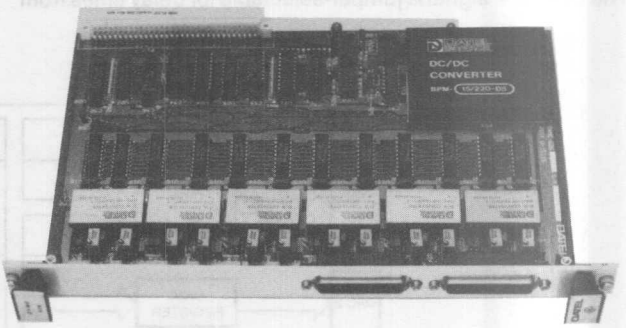
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DVME-626
16-Bit, 6-Channel VMEbus D/A Board

FEATURES

- 6 D/A channels
- 16-Bit resolution
- 14-Bit monotonicity
- Designed to meet precision servo control requirements
- Complete hardware-compatible with VMEbus specifications
- 25 µseconds settling time
- Available in two models:
  DVME-626V1 for ±10V dc output
  DVME-626V2 for 0 to +10V dc and ±5V dc outputs
- Three input coding types:
  A. Bipolar 2's complement
  B. Bipolar offset binary
  C. Unipolar straight binary
- Up to 0.005% full-scale range accuracy
- ±0.005% of full-scale range differential nonlinearity
- On-board dc-to-dc power converter supplies ±15V dc for internal logic circuits



The DVME-626 is DATEL's high resolution VMEbus-based D/A board that provides analog outputs for up to 6 channels. The 16-bit D/A board is designed to deliver exceptionally high-performance in rugged industrial environments. The 14-bit monotonicity and 0.005% FSR accuracy makes the board an ideal choice for precision servo control and similiar applications. The DVME-626 is supported by MS-DOS software for calibration and diagnostics.

GENERAL DESCRIPTION

The DVME-626 is a D/A member of DATEL's VMEbus family. The board delivers precision and performance that makes it easily acceptable for various test and control applications. On-board hardware resources provide 6 high-resolution analog outputs with an accuracy of better than 0.005% of full-scale range. The DVME-626 accepts 16-bit digital data, coded in bipolar 2's complement, bipolar offset binary, or unipolar straight binary. The board is rigorously tested under extreme environmental conditions to meet DATEL's stringent quality assurance requirements.

The DVME-626 easily fits into a VMEbus card cage and is addressable using short I/O space address lines. The on-board switches select the base address of the board. Functions relating to input data coding and output voltage range are easily selectable using jumpers.

Functionally, the DVME-626 consists of a VMEbus interface section and a digital-to-analog converter (DAC) section. The DAC data register section contains a data register and D/A converter for each section. One unique feature of the DVME-626 is that the DAC outputs will reset to 0.000V during reset, regardless of whether unipolar or bipolar outputs are selected. Figure 1 shows the functional block diagram of the board.

The DVME-626 D/A board will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the board. The user's manual also contains information on troubleshooting the board.

The board is shipped with an example 68010 assembly language diagnostic program on a 5 1/4" floppy diskette, formatted for the MS-DOS operating systems. Consult the factory regarding the availability of the diagnostic program's source code on other disk formats.

ORDERING INFORMATION

DVME-626V —
- 1 — ± 10V dc output range
- 2 — 0 to 10V and ±5V dc output ranges

VMEbus Interface

The DVME-626 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-626 generates the data acknowledge (DTACK *) signal to notify acceptance of data from the VMEbus data lines, D00 through D15. The DTACK * signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host CPU response times.

The interface logic decodes the VMEbus control lines WRITE *, DS0 *, DS1 *, and SYSRESET * to select and control the interface. These signals control the board select and the VMEbus transfer functions. The DVME-626 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

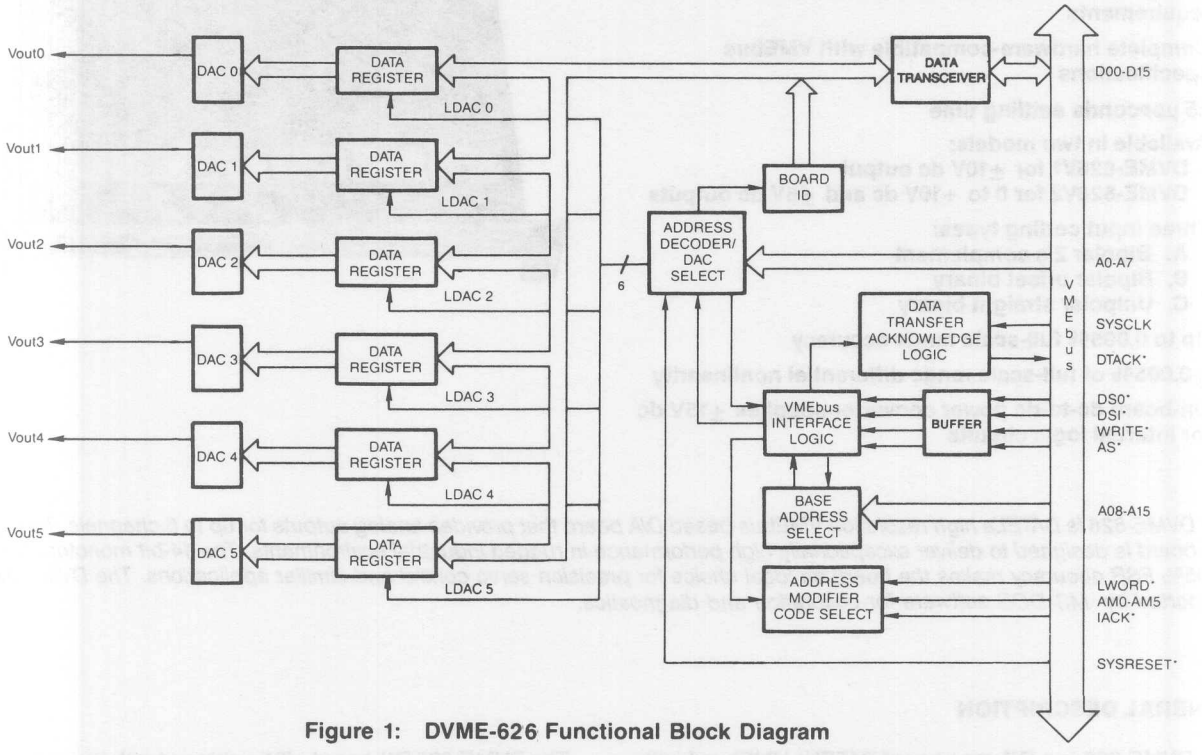


Figure 1: DVME-626 Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, unless otherwise noted)

INTERFACE SPECIFICATIONS

Data Bus . . . . . 16 Bits (A16:D16 slave)

Address Bus . . . . . Short I/O Space; 16 address lines

Address Modifier Codes . . . . . Codes used 29H, 2DH, 39H, and 3DH

Memory Mapping . . . . . Short I/O space, user or supervisor, 256 words allocated per board.

Data Transfer . . . . . DTACK * signal line. Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines.

Note: The VMEbus SYSCLK signal is required.

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector . . . . . 96-pin male DIN connector.

J1 and J2 Analog Output Connectors . . . . . 25-pin D-type female connector, DB-25S

ANALOG SPECIFICATONS

ANALOG OUTPUT

Number of Channels . . . . . 6, non-isolated

Output Range
DVME-626V1 . . . . . ±10V dc
DVME-626V2 . . . . . 0 to 10V and ± 5V dc

Digital Input Coding . . . . . Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary
(jumperable)

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Resolution . . . . . 16 Bits

Monotonicity . . . . . 14 bits

Reset . . . . . Output resets to 0.000V dc at power-on

Accuracy . . . . . 0.005% of FSR, minimum

Differential nonlinearity . . . . . 0.005% of FSR, maximum

Zero temperature drift . . . . . 5 ppm/°C, typical

Offset temperature drift . . . . . 8 ppm/°C, typical

Gain temperature drift . . . . . 20 ppm/°C, typical

Settling time . . . . . **25 µseconds (small step)**

Output current . . . . . ±5 mA, typical

Output impedance . . . . . 50 milliohms, typical

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 3.0 Amperes, typical

Power Supply Rejection . . . . . ±0.002%, typical

PHYSICAL CHARACTERISTICS

Outline Dimensions . . . . . 9.19″ W×6.3″ D×0.6″ H (233.35×160×15.24 mm)

Weight . . . . . 1 lb. (453.6 grams)

Operating Temperature Range . . . . . 0 to +60° C Range

Storage Temperature Range . . . . . –20 to +80° C Range

Humidity . . . . . 0 to 90%, non-condensing

DVME-626 PROGRAMMING INFORMATION

The DVME-626 contains six programmable registers that store digital data for each 16-bit D/A converter. The board responds only to word data transfers on write operations. Table 1 shows the addresses of the identification code and the registers. Figure 2 shows the format of the DAC data register.

Table 1: DVME-626 Register Locations.

ADDRESS	FUNCTION	CONTENTS
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 160	Write	D/A Channel 0
Base + 162	Write	D/A Channel 1
Base + 164	Write	D/A Channel 2
Base + 166	Write	D/A Channel 3
Base + 168	Write	D/A Channel 4
Base + 170	Write	D/A Channel 5

Word Address: Base + 160, Base+162, Base+164, Base+166, Base + 168, and Base + 170

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	DA13	DA14	DA15	DA16
MSB															LSB

Figure 2: DVME-626 DAC Data Register Format

I/O CONNECTIONS

The DVME-626 D/A boards provide front panel J1 and J2 connectors for analog output connections. Tables 2 and 3 list the output signals of the J1 and J2 connectors respectively.

Table 2: DVME-626 ANALOG OUTPUT CONNECTOR J1

PIN #	DESCRIPTION
1	DAC 0 V OUT
2	NO CONNECTION
3	NO CONNECTION
4	DAC 1 V OUT
5	NO CONNECTION
6	NO CONNECTION
7	DAC 2 V OUT
8	NO CONNECTION
9	NO CONNECTION
10	DAC 3 V OUT
11	NO CONNECTION
12	NO CONNECTION
13	NO CONNECTION
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	NO CONNECTION
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	NO CONNECTION
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	NO CONNECTION
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	NO CONNECTION

Table 3: DVME-626 ANALOG OUTPUT CONNECTOR J2

PIN #	DESCRIPTION
1	DAC 4 V OUT
2	NO CONNECTION
3	NO CONNECTION
4	DAC 5 V OUT
5	NO CONNECTION
6	NO CONNECTION
7	NO CONNECTION
8	NO CONNECTION
9	NO CONNECTION
10	NO CONNECTION
11	NO CONNECTION
12	NO CONNECTION
13	NO CONNECTION
14	DAC 4 ANALOG RETURN
15	DAC 4 ANALOG RETURN
16	NO CONNECTION
17	DAC 5 ANALOG RETURN
18	DAC 5 ANALOG RETURN
19	NO CONNECTION
20	NO CONNECTION
21	NO CONNECTION
22	NO CONNECTION
23	NO CONNECTION
24	NO CONNECTION
25	NO CONNECTION

DVME-626 Board Identification Code

Byte Address	ASCII Code	FUNCTION
Base + 1 Base + 3 Base + 5 Base + 7 Base + 9	V M E I D	Identifier. This ASCII code is present for all DATEL VMEbus boards
Base + 0B Base + 0D Base + 0F	D A T	Manufacturer ID. DAT is the ID for DATEL
Base + 11 Base + 13 Base + 15 Base + 17 Base + 19 Base + 1B Base + 1D Base + 1F	d V M E – 6 2 6	Board model number

DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base+0 through Base+63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base+64 through Base+77	DVME-660	48 line digital I/O board
Base+78 through Base+127		Not Used
Base+128 through Base+143	DVME-611	DVME-611: 32 single-ended/ 16 differential channel A/D board
	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base+144 through Base+151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples, RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base+152 through Base+159		Not Used
Base+160 through Base+175	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
	DVME-624	DVME-624: 4-channel isolated board
	DVME-626	DVME-626: 6-channel 16-bit D/A board
	DVME-628	DVME-628: 8-channel 12-bit D/A board
Base+176 through Base+191		Not Used
Base+192 through Base+255		Not Used

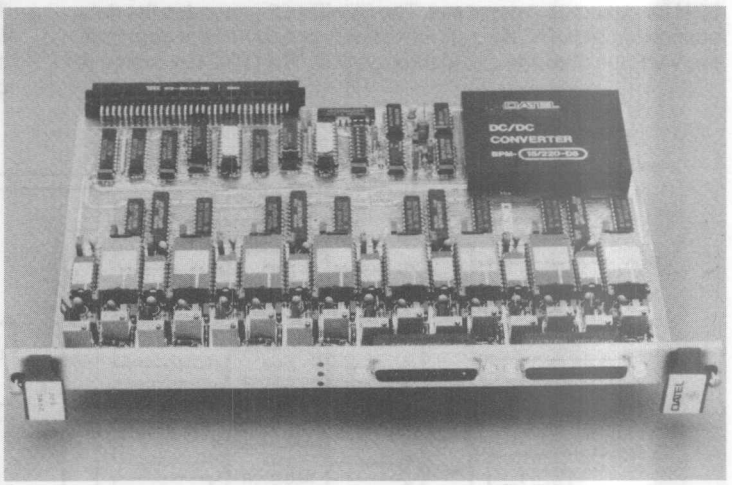
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DVME-628
12-Bit, 8-Channel VMEbus D/A Board

FEATURES

- 8 D/A channels
- 12-Bit resolution
- Complete hardware-compatible with VMEbus specifications.
- 6 μSecond settling time.
- Three types of input coding:
  - A. Bipolar 2's complement
  - B. Bipolar offset binary
  - C. Unipolar straight binary
- Five output voltage ranges:
  - A. 0 to +5V dc
  - B. 0 to +10V dc
  - C. ±2.5V dc
  - D. ±5V dc
  - E. ±10V dc
- Up to 0.05% full-scale range accuracy.
- ±1/2 LSB differential nonlinearity
- 4-to-20 mA current loop output capability for DVME-628C model.
- On-board dc-to-dc power converter supplies ±15V dc for internal logic circuits.



The DVME-628 is DATEL's high-end, VMEbus-based D/A board that provides analog output for up to 8 channels. The 12-bit D/A board, with 6 microsecond settling time, is designed to deliver high-performance in process control, test instrumentation and similar applications. The three input coding schemes and five analog output voltage ranges makes the board an ideal choice for the most industrial applications.

GENERAL DESCRIPTION

DATEL's VMEbus family of boards offer a complete solution to various data acquisition applications. The DVME-628 is the D/A member of this family, providing up to 8 analog outputs for the host VMEbus system. The D/A board offers a resolution of 12 bits and operates with an accuracy of beter than 0.05% of full-scale range. The board is rigorously tested under extreme environmental conditions for DATEL's stringent quality assurance requirements.

The DVME-628 easily fits into a VMEbus card cage and is addressable using short I/O space address lines. The on-board switches select the base address of the board. Functions relating to input data coding and output voltage range are easily selectable using jumpers.

Functionally, the DVME-628 consists of a VMEbus interface section and a digital-to-analog conveter (DAC) section. The DAC data register section contains a data register and D/A converter for each section. For DVME-628C models the DAC section also contains voltage to 4-to-20 mA current loop conversion logic for each channel. One unique feature of the DVME-628 is that the DAC outputs will reset to 0.000V during reset regardless of whether unipolar or bipolar outputs are selected.

The DVME-628 D/A board will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the board. The user's manual also contains information on troubleshooting the board.

The board is shipped with an example 68010 assembly language diagnostic program on a 5 1/4" floppy diskette, formatted using VERSAdos. The diagnostic program source code is available in hard copy from DATEL. Consult the factory regarding the availability of the diagnostic program's source code in other disk formats.

ORDERING INFORMATION

DVME-628
- V - Voltage outputs only
- C - Voltage and 4-to-20mA current loop outputs

VMEbus Interface

The DVME-628 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-628 generates the data acknowledge (DTACK★) signal to notify acceptance of data from the VMEbus data lines, D00 through D15. The DTACK★ signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.
The interface logic decodes the VMEbus control lines WRITE ★, DS0 ★, DS1 ★, and AS ★ to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-628 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

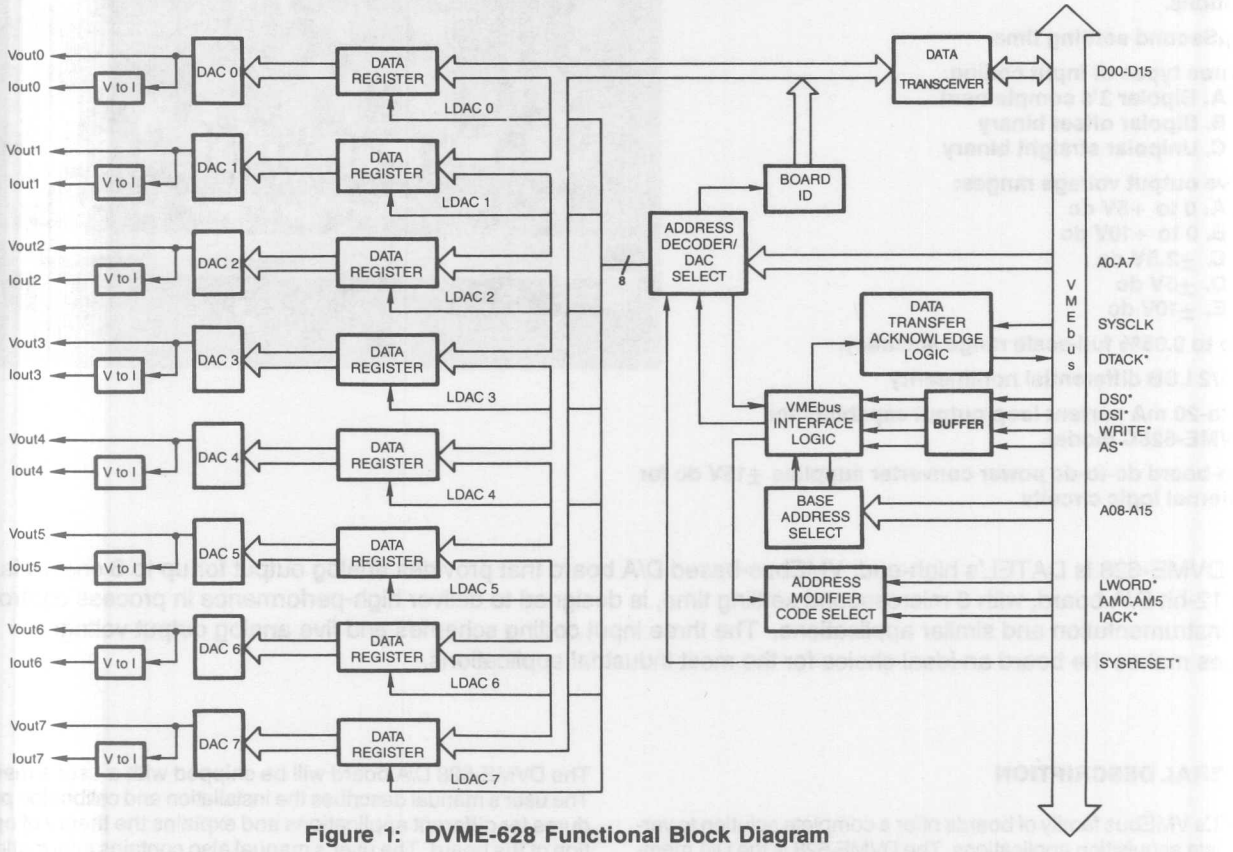


Figure 1: DVME-628 Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, unless otherwise noted)

Interface specifications

Data Bus.....16 Bits (A16:D16 slave)

Address Bus.....Short I/O Space; 16 address lines

Address Modifier Codes.....Codes used 29H, 2DH, 39H, and 3DH

Memory Mapping.....Short I/O space, user or supervisor, 256 words allocated per board

Data Transfer.....DTACK ★ signal line. Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector.....96-pin male DIN connector

J1 and J2 Analog Output Connectors.....25-pin D-type female connector.

ANALOG SPECIFICATONS

ANALOG OUTPUT

Number of Channels.....8 non-isolated, single-ended

Output Range.....0 to +5V dc
0 to +10V dc
± 2.5V dc
± 5V dc
± 10V dc

Digital Input Coding.....Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary

NOTE: The VMEbus SYSCLK signal is required.

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Resolution . . . . . 12 Bits

Reset . . . . . Output resets to 0.000V dc at power-on

Accuracy . . . . . 0.05% of FSR, minimum

Differential . . . . . 0.5 LSB, maximum non-linearity

Zero Temperature Drift . . . . . 3 ppm/ °C, typical
5 ppm/ °C, maximum

Offset Temperature Drift . . . . . 5 ppm/ °C, typical
10 ppm/ °C, maximum

Gain Temperature Drift . . . . . 15 ppm/ °C, typical
30 ppm/ °C, maximum

Settling Time . . . . . 6 μSeconds, maximum

Output Current . . . . . ±5 mA, typical

Output Impedance . . . . . 50 milliohms, typical

CURRENT LOOP

Current Loop . . . . . 4-to-20 mA, conforming to ISA Standard 550.1, Type 4, Class U

Accuracy . . . . . 0.1% of FSR, minimum

Excitation . . . . . +15V dc, minimum
(User-supplied) . . . . . +24V dc, typical
+36V dc, maximum

Load Resistance . . . . . 100 Ohms, minimum
1000 Ohms, maximum

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at . . . . . 2.0 Amperes, typical
2.3 Amperes, maximum

PHYSICAL CHARACTERISTICS

Outline Dimensions . . . . . 9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)

Weight . . . . . 1 lb. (453.6 grams)

Operating Temperature Range . . . . . 0 to +60 °C

Storage Temperature Range . . . . . -20 to +80 °C

Humidity . . . . . 0 to 90%, non-condensing

DVME-628 PROGRAMMING INFORMATION

The DVME-628 contains eight programmable registers that store digital data for the D/A converters. The board responds only to word data transfers on write operations. Since the DVME-628 uses 12-bit D/A converters, the 12 most significant bits of the DAC data registers are used for conversion. Table 1 shows the addresses of the identification code and the registers. Figure 2 shows the format of the DAC data register.

Table 1: DVME-628 Register Locations

ADDRESS	FUNCTION	CONTENTS
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 160	Write	D/A Channel 0
Base + 162	Write	D/A Channel 1
Base + 164	Write	D/A Channel 2
Base + 166	Write	D/A Channel 3
Base + 168	Write	D/A Channel 4
Base + 170	Write	D/A Channel 5
Base + 172	Write	D/A Channel 6
Base + 174	Write	D/A Channel 7

Word Address: Base + 160, Base + 162, Base + 164, Base + 166, Base + 168, Base + 170, Base + 172, and Base + 174

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x
MSB											LSB				

Figure 2: DVME-628 DAC Data Register Format

OUTPUT CONNECTIONS

The DVME-628 D/A boards use the J1 and J2 connectors for analog output connections. Tables 2 and 3 list the output signals of the J1 and J2 connector respectively.

Table 2: DVME-628 Analog Output Pinout Details (J1)

PIN #	DESCRIPTION
1	DAC 0 V OUT
2	DAC 0 I LOOP
3	DAC 0 V LOOP
4	DAC 1 V OUT
5	DAC 1 I LOOP
6	DAC 1 V LOOP
7	DAC 2 V OUT
8	DAC 2 I LOOP
9	DAC 2 V LOOP
10	DAC 3 V OUT
11	DAC 3 I LOOP
12	DAC 3 V LOOP
13	NO CONNECTION
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	NO CONNECTION
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	NO CONNECTION
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	NO CONNECTION
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	NO CONNECTION

Table 3: DVME-628 Analog Output Pinout Details (J2)

PIN #	DESCRIPTION
1	DAC 4 V OUT
2	DAC 4 I LOOP
3	DAC 4 V LOOP
4	DAC 5 V OUT
5	DAC 5 I LOOP
6	DAC 5 V LOOP
7	DAC 6 V OUT
8	DAC 6 I LOOP
9	DAC 6 V LOOP
10	DAC 7 V OUT
11	DAC 7 I LOOP
12	DAC 7 V LOOP
13	NO CONNECTION
14	DAC 4 ANALOG RETURN
15	DAC 4 ANALOG RETURN
16	NO CONNECTION
17	DAC 5 ANALOG RETURN
18	DAC 5 ANALOG RETURN
19	NO CONNECTION
20	DAC 6 ANALOG RETURN
21	DAC 6 ANALOG RETURN
22	NO CONNECTION
23	DAC 7 ANALOG RETURN
24	DAC 7 ANALOG RETURN
25	NO CONNECTION

DVME-628 BOARD IDENTIFICATION CODE

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	2	
+ 1F	8	

DATEL VMEbus Short I/O Memory Organization*

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

*This chart does not apply to the following products:

DVME-601
DVME-613
DVME-614
DVME-622
DVME-630

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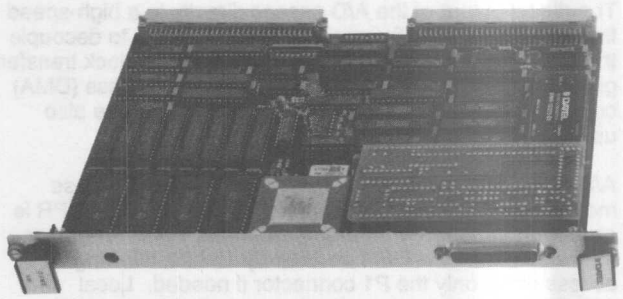
DATEL®
INNOVATION and EXCELLENCE

DVME-630
Very High Speed VME bus A/D-DSP Coprocessor Board

FEATURES

- **Up to 10MHz A/D sample rate**
- **Choice of 12 or 14-bit A/D resolution**
- **Up to 16SE/8D analog input channels**
- **512Kb dual-ported RAM, 1Mb and 4Mb optional**
- **Two 1k x 32 internal DSP RAM**
- **8k x 32 Expansion (secondary) RAM**
- **2, 4, and 8-channel simultaneous sampling**
- **Local TMS320C30 digital signal processor 32/40MHz**
- **On-board DSP library - FFT's, filters, matrix math, etc.**
- **Fast, simple, powerful command Executive**
- **No local programming required.**
- **Vectored interrupt to VME bus host**
- **Supports VME16 and VME32 transfers**
- **Analog output and digital I/O support**

10MHz Sampling!



DESCRIPTION

Advanced performance from the DVME-630's on-board Digital Signal Processor (DSP) supports a broad range of high-speed waveform analysis and recording applications. The DVME-630 will acquire up to sixteen analog input channels, digitize them and store them in local memory while DSP math processing and data transfer is done concurrently. The system is intended for preprocessing "seamless" A/D data streams to the host system.

The DVME-630 is ideal for non-stop, continuous Fast Fourier Transform (FFT) processing, communications receiver signal collection to disk or simultaneous graphics display of spectral data. Application areas include signal recovery from noisy channels, harmonic distortion analyzers, and vibration/ resonance filtering systems. For use with ultrasonic, sonar or acoustic signals, the interrupt-driven, simultaneous block transfers of data ensure no information loss. Other uses include high-speed mapping and imaging, satellite channels, astrophysics, seismology, biomedical signals, array processing, control systems, simulators, engine analyzers, aerodynamics and vehicle systems.

The board consists of a pluggable analog input subsection, timer-counters, DSP central processing unit (CPU), dual port RAM, local RAM, bus interface, registers and DC power supply. Input signals pass through a very high speed channel multiplexer (except model DVME-630D,F,G, and J) to a sampling analog-to-digital (A/D) converter. On models DVME-630A, F, G, and J an A/D converter per channel allows two to eight channels to be acquired simultaneously. A choice of channels, input ranges, speeds and resolution is offered in the analog section.

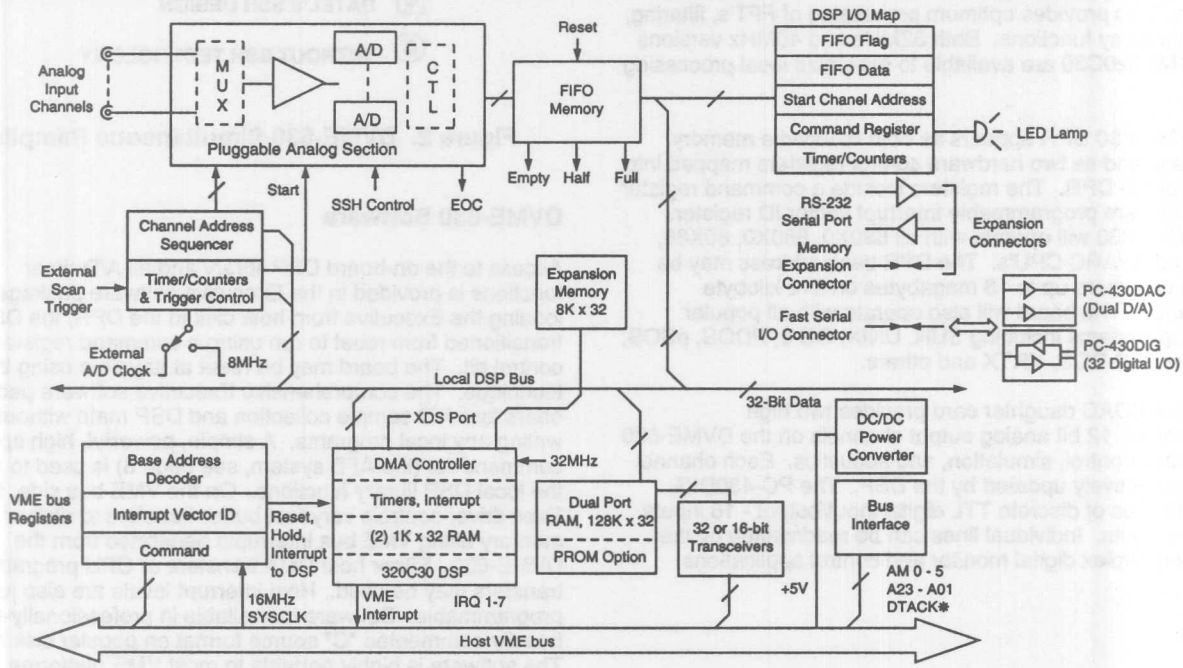


Figure 1. DVME-630 Block Diagram

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MS-DOS is a Microsoft trademark

A/D triggering for spectral and FFT applications must be precisely controlled. This is handled by a programmable timer-counter section which can control the interval between A/D conversions and the interval between multi-sample A/D scans. The number of samples may also be counted for repeating array sampling. The timer-counter may use an on-board crystal oscillator or an external timebase for precision phase-tracking.

The digital output of the A/D passes directly to a high-speed first-in, first-out (FIFO) memory. The FIFO acts to decouple the precision timing of the A/D section with the block transfers governed by the DSP internal direct memory access (DMA) controller. Additional timers internal to the DSP are also used.

A/D FIFO data may be sent to dual port random access memory (DPR) shared with the host VME bus. The DPR is organized as 128k by 32 bits of fast static RAM. The user may also set up the DPR as 256k by 16 bits, allowing all access using only the P1 connector if needed. Local A/D-FIFO block transfers may be controlled by the DMA controller in the DSP. The DMA may run in background while math processing continues. Local FIFO and DMA TC interrupts to the DSP arbitrate these activities. Typically, a swapped dual buffer method is used so that samples are not lost during other processing. Local hardware registers control all A/D, FIFO and trigger activity. Local DSP memory capacity may be increased by an additional 1 or 4 megabytes using DATEL's MEM-30 daughter modules.

Single cycle fetch and execution, parallel instructions, zero-overhead of looping instructions, software variable wait-states, block repeat and a 64-word internal instruction cache memory are some of the advanced high speed features of the Texas Instruments 320C30 DSP. The DSP uses 32-bit local data paths for very high speed. Simultaneous access attempts to the DPR by both the VME bus host and the DSP are resolved by high speed arbitration logic. The DSP also has a separate 8k by 32-bit local expansion memory for the stack or temporary data. The architecture of the DSP allows simultaneous processing of two tables from two sections of memory. This provides optimum processing of FFT's, filtering, and other array functions. Both 32MHz and 40MHz versions of the TMS320C30 are available to maximize local processing power.

The DVME-630 DPR appears as both read/write memory addresses and as two hardware control registers mapped into the top of the DPR. The registers include a command register and a software programmable interrupt vector ID register. The DVME-630 will operate with all 680X0, 880X0, 80X86, RISC and SPARC CPU's. The DPR base address may be located anywhere up to 16 megabytes on 512 kilobyte boundaries. The board will also operate with all popular operating systems including SUN, UNIX, OS-9, PDOS, pSOS, VxWorks, MS-DOS, VRTX and others.

The PC-430DAC daughter card provides two high performance, 12 bit analog output channels on the DVME-630 for process control, simulation, and acoustics. Each channel can be selectively updated by the DSP. The PC-430DIG offers 32 lines of discrete TTL digital input/output - 16 inputs and 16 outputs. Individual lines can be read/written by the DSP for complex digital monitor and control applications.

Simultaneous Sample/Hold

As shown in Figure 2, four input signals are sampled at the same time using the DVME-630A's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired simultaneously they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors from conventional multiplexer scanning. The DVME-630F, G, and J employ a similar technique at higher speed using two simultaneous A/D's. The DVME-630J uses 8 simultaneous A/D's.

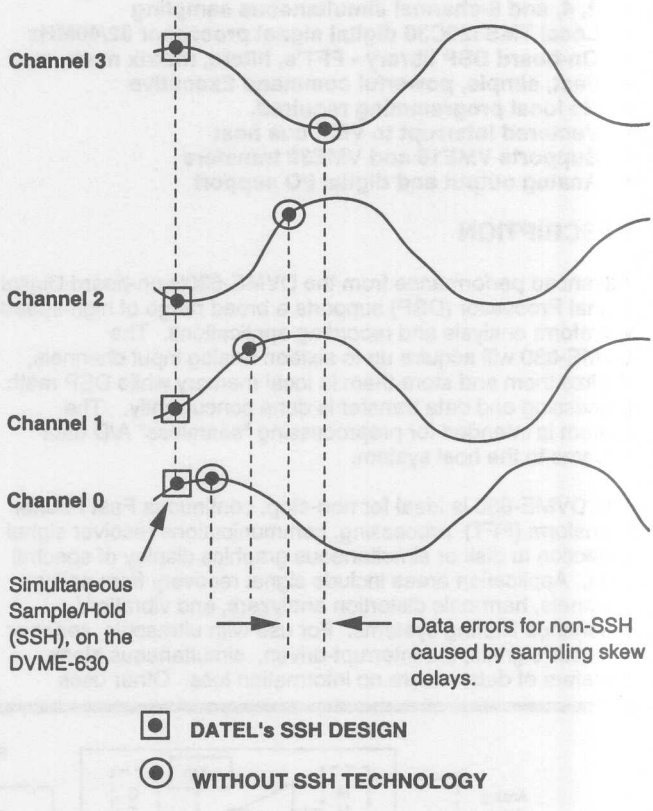


Figure 2. DVME-630 Simultaneous Sampling

DVME-630 Software

Access to the on-board DSP library and all A/D-timer functions is provided in the Executive software package. After loading the Executive from host disk to the DPR, the DSP is transitioned from reset to run using a command register control bit. The board may be reset at any time using this technique. The comprehensive Executive software package offers fast A/D sample collection and DSP math without writing any local programs. A simple, powerful, high speed command list (the AFB system, see page 8) is used to access the local DSP library functions. On the VME bus side, the Exec driver controls very fast buffer transfers to disk or memory using VME bus interrupts generated from the DVME-630. Either host DMA transfers or CPU program transfers may be used. Host interrupt levels are also jumper programmable. Software is available in professionally-written, heavily-commented "C" source format on popular disk media. The software is highly portable to most VME platforms.

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FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	DVME-630A	DVME-630B	DVME-630C	DVME-630D	DVME-630E
Number of Channels	4 Simul.	4	4	1	16SE/8D
Input Configuration (non-isolated)	Single-Ended	Single-Ended	Single-Ended	Differential	SE or Diff.
Full Scale Input Ranges (user-selectable, gain = 1) [Footnote 1]	0 to +10V ±10V	0 to +10V ±10V ±5V	0 to +10V ±10V ±5V	±5V	0 to +10V ±10V ±5V
Input Bias Current	±1nA	±1nA	±1nA	±1nA	±1nA
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	2µs	2µs	2µs
Common Mode Voltage Range, maximum	—	—	—	±1V	±10V
Input Impedance [Footnote 2]	10MΩ	10MΩ	10MΩ	2kΩ	100MΩ
SAMPLE/HOLD					
Acquisition Time (FSR step, to 0.01% of FSR, max.)	900ns	750ns	200ns	50ns	750ns
Aperture Delay	15ns	20ns	20ns	10ns	20ns
Aperture Delay Uncertainty	±8ps	±100ps	±40ps	±7ps	±40ps
A/D CONVERTER					
Resolution	12 bits	14 bits	12 bits	12 bits	12 bits
Conversion Period	500ns	1.6µs	500ns	200ns	500ns
SYSTEM DC CHARACTERISTICS					
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1	±2	±1
Differential Non-linearity (LSB of FSR)	±0.75	±1	±0.75	±1	±0.75
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.1	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±0.1	±0.3	±0.1
SYSTEM DYNAMIC PERFORMANCE [Footnote 3]					
Input Bandwidth (single channel, FSR input) [Footnote 10]	1MHz	200kHz	1MHz	2.5MHz	200kHz
Throughput to FIFO (single channel, gain = 1)	1.5MHz	500kHz	1.6MHz	5MHz [6]	2MHz
Throughput to FIFO (sequential channels, gain = 1) [Footnotes 4 & 8]	1MHz	330kHz	500kHz	—	500kHz
Total Harmonic Distortion [Footnote 5]	–72dB	–75dB	–72dB	–68dB	–72dB

ANALOG INPUTS	
Programmable Gains	See Footnote 1
Common Mode Rejection (DC - 60Hz)	-80dB (g = 100) (630E)
Addressing Modes	1. Single channel 2. Simultaneous sampling 3. Sequential with autosequenced addressing 4. Random addressing by software

A/D CONVERTER	
Output Coding	Positive-true, right-justified, straight bin. (unipolar) or right-justified 2's comp. (bipolar) with sign extension thru bit 15
Trigger Sources (Software selectable)	1. Local pacer frame clock 2. External TTL frame clock
A/D Sample Clock	1. Internal programmable 82C54 timer 2. Ext. TTL input, active high

FUNCTIONAL SPECIFICATIONS CONTINUED

(Typical at +25°C, dynamic conditions, gain = 1, unless noted.)

ANALOG INPUTS	DVME-630F	DVME-630G	DVME-630H	DVME-630J
Number of Channels	2 simul.	2 simul.	1	8 simul.
Input Configuration (non-isolated)	Single-Ended	Single-Ended	Differential	Single-Ended
Full Scale Input Ranges (user-selectable, gain = 1) [Footnote 9]	0 to +10V ±5V	±5V 0 to +10V (special order)	±5V (other ranges special order)	0 to +2.5V ±5V, ±10V (separate unipolar & bipolar models)
Input Bias Current	±1nA	±1nA	—	±50nA (unipolar version)
Input Overvoltage (no damage, power on)	±15V	±15V	±15V	±15V
Overvoltage Recovery Time, maximum	2µs	2µs	1µs	—
Common Mode Voltage Range, maximum	—	—	±1V	—
Input Impedance [Footnote 2]	1kΩ	1MΩ	2kΩ	8kΩ (bipolar)
SAMPLE/HOLD				
Acquisition Time (FSR step, to 0.01% of FSR, max.)	165ns	350ns [11]	35ns	400ns
Aperture Delay	20ns	20ns	10ns	—
Aperture Delay Uncertainty	±40ps	±70ps	±3ps RMS	—
A/D CONVERTER				
Resolution	12 bits	14 bits	12 bits	12 bits
Conversion Period	400ns	500ns*	100ns [Footnote 7]	2µs (all chans. in simul. sampling)
SYSTEM DC CHARACTERISTICS				
Integral Non-linearity (LSB of FSR)	±1	±1.5	±1.5	±1 max.
Differential Non-linearity (LSB of FSR)	±1	±1	±1	±1 max.
Full Scale Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 9]
Zero or Offset Temperature Coefficient (LSB per °C)	±0.1	±0.3	±1	[Footnote 9]
SYSTEM DYNAMIC PERFORMANCE				
Input Bandwidth (single channel, FSR input) [Footnote 10]	1MHz	500kHz	5MHz	100kHz
Throughput to FIFO (single channel, gain = 1)	2MHz	1MHz*	10MHz [7]	400kHz
Throughput to FIFO (sequential channels, gain = 1) [Footnotes 4 & 8]	4MHz (2 chans.)	2MHz* (2 chans.)	—	250kHz/chan. (8 chans. simul.)
Total Harmonic Distortion [Footnote 5]	–70dB	–80dB	–65dB	–77dB

*Dual 2MHz 14-bit sampling is available on special order.

FOOTNOTES

1. Resistor-programmed gain from x1 to x100 is available on the DVME-630E with increased settling delay at higher gains. Fixed gains of x1 and x10 on 2 channels, offering 1V ranges, are user selectable on the DVME-630A.
2. The input impedance of 10 megohms minimum avoids attenuation errors from external input source resistance. For many applications, an in-line coaxial 50Ω shunt, inserted adjacent to the front connectors, is recommended to reduce line reflections and standing wave errors. Input impedance is shown with power on. Impedance with power off is 1500Ω or less.
3. Allow 20 minutes warmup time to rated specifications for models DVME-630B,G.
4. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion and FIFO transfer. The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the DVME-630C were scanned, the maximum sample rate on any one channel would be 1 microsecond X 4 channels = 4 microseconds (250kHz per channel).

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TRIGGER CONTROL	
Programmable Timer Functions	82C54 (DSP waits required) 1. A/D sample counter. 2. A/D start rate (16 bit divisor) 3. SSH sample counter (630A)
Pacer Sample Counter	3 to 65,536 samples. Drives the Acquire flag gate for A/D start pulses. Larger sample blocks may be programmed.
Timer Clock Source (User-selectable)	1. Internal 8MHz crystal clock 2. External TTL input, 10MHz max.
Trigger	Starts an A/D frame. Programmable via DSP CLK.

LOCAL MICROCOMPUTER	
CPU Type	Texas Instruments TMS 320C30 Digital Signal Processor
Local Data Bus	32 bits
CPU Clock Speed	32MHz and 40MHz
Local DMA Controller	Internal to 320C30 CPU
Primary Memory	512kb SRAM, shared with VME
Local Memory Expansion	1Mb (MEM-30), 4Mb (MEM-30B)
PROM Option	32k x 32 of primary memory may be replaced by user-programmed Read Only Memory.
Expansion Memory	8k x 32 static RAM (no host access)
Internal DSP Memory	Two 1k x 32
Dual Port Access from VME bus	Hold mode by control bit or dynamic hold per each access.
CPU Test Port	Supports TI XDS1000 Extended Development System.
Local DSP Interrupts	Int 0-3 from VME host request, A/D FIFO or sample count acquire flags or optional external interrupt.
Wait States	May be software programmed via DSP register up to 7 waits.

VME bus INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Data Bus Width	16 bits using P1 connector or 32 bits using P1 and P2. Changed by alternate transceiver sockets on board.
Address Bus	24 address lines (A23-A1) plus 6 Address Modifiers.
Address Modifier Codes	39 hex or 3D hex, selectable.
VME bus Interrupt	1 line, selectable IRQ 1-7*. Asserts maskable programmable 8-bit vector ID code.
VME bus Interrupt Source	DSP I/O bit (software programmable).
Architecture	SAD24:SD16 or SAD24:SD32 memory-mapped slave consisting of 128k x 32-bit longwords of dual access RAM. The DVME-630 is not a bus master.
Control/Status Functions	DSP halt request, DSP reset/run, VME interrupt enable/disable, vector ID R/W, force local maskable interrupt to DSP.
Data Transfer	Uses 16MHz VME bus SYSCLK signal (required) to generate DTACK* with PAL programmed delay in 62.5ns steps. Will accept host DMA controller access.

CONNECTORS	
VME bus, P1 and P2	Two 96-pin male DIN connectors.
Analog Input Connect	DB-25S female type, includes the A/D trigger input
Memory Expansion (32-bit data)	72-pin header, unbuffered. Uses 0.025" square pins, 0.100" spacing, see MEM-30 data sheet.
XDS CPU Port	12-pin header, 0.1" pinning.
Fast CPU Serial I/O (Incl. trigger, clock, etc.)	20-pin header, unbuffered, 0.1" pinning. Can plug PC-430DIG (analog out) or PC-430DAC (digital I/O) modules onto this connector.
RS-232-C Asynch. Serial Port	3-pin header (Xmt, Rcv, Gnd), 0.1" pinning. Uses software UART.

MISCELLANEOUS	
LED Lamp	Front panel green LED lamp may be controlled by internal register.
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain per channel for SSH on DVME-630A, F, and G. A single offset and gain pot is provided on DVME-630B,C,D,E. Model DVME-630J is auto calibrating. Recommended recalibration interval is 90 days in stable conditions.
Power Required	+5V dc ±5% at 4Amps max. from VME bus.
Operating Temp Range	0 to +60°C. Forced cooling is recommended.
Storage Temp Range	-20 to +85°C
Relative Humidity	10% to 90%, non-condensing.
Altitude	0 to 10,000 feet.
Outline Dimensions	Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233,5 x 160 x 15,24 mm).
Weight	22 ounces

FOOTNOTES Cont.

5. THD test conditions are:
   1. Input frequency: 500kHz (630A,F), 300kHz (630C), 100kHz (630G), 200kHz (630B,E), 1MHz (630D), 2MHz (630H)
   2. Generator/filter THD is -90dB minimum.
   3. THD computed by FFT to 5th harmonic.

$$THD = 20 \log_{10} \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}$$

   4. Inputs are –0.5dB full scale. No channel advance.
   5. A/D trigger rate = 1.5MHz (630A), 500kHz (630B,C,E), 4MHz (630D), 2MHz (630F), 1MHz (630G), 10MHz (630H)

6. DVME-630D: 5MHz sampling requires an external A/D clock. Maximum on-board sampling is 4MHz.

7. DVME-630H: 10MHz sampling requires an external A/D clock *and* must bypass the 82C54 timer. Contact factory for details. 10MHz sampling may continue until the FIFO memory is full.

8. The DVME-630F,G, and J operate in single-channel random address mode or multichannel with automatic channel sequencing. *All* multichannel autosequential models continuously wrap the channel address back to channel zero without delay.

9. DVME-630J: models are dedicated as unipolar (0 to +2.5V) or bipolar (±5V, ±10V) input ranges. Other input ranges are available on special order. Pretrimmed gain and offset/zero errors are ±4LSB max. each over temperature range. Monotonicity: no missing codes over temp. range.

10. Full power bandwidth is shown at approximately 3% distortion level. This is not the –3dB amplitude response which is at a higher but non-Nyquist frequency.

11. DVME-630G acquisition time is 350ns to ±0.003% of FSR.

DVME-630 Control

The following are some methods to control the DVME-630:

- Use the DVME-630 Executive Software (DVME-630EXEC)
- Modify the Executive by adding own code (DVME-630EXEC/SRC)
- Develop your entire application using the TI compiler - don't use DVME-630EXEC/SRC
- Use a third party TMS320C30 operating system, such as Spectron's SPOX and adapt it to the DVME-630

Executive Software

The complete Executive software package is an integrated environment for full control of the DVME-630. It includes programs which run on both the host VME bus and the DVME-630. The Executive package consists of:

The AFB ASCII to binary file converter (PARSE).
A small menu shell.
The VME bus Host package (DVME-630SET.C).
The Executive scheduler, DSP library, boot code, vectors and full local DVME-630 system (SKED.OUT).

To use this environment, the user simply converts the AFB text file to a binary file, downloads this to the DVME-630 scheduler and retrieves data files. Once the configuration is saved, an application can be executed from one command line or from a batch file.

DVME-630 Host System Architecture

When the DVME-630 is fully installed, the host VME memory map contains the device driver, the Interrupt Service Routine, a small menu program and the DVME-630's dual port RAM. These systems all work together to provide fast disk or buffer transfers of DSP'd A/D data. The entire system is controlled by simple user-written command files. Figure 4 illustrates the host system architecture.

The primary function of the EXEC is a high speed disk data recorder. Data may be all sent to memory first (high speed) then saved to disk. Or data may be sent directly to disk (large capacity).

VME Host Driver

The final portion of the full Executive package is the Driver containing a library of functions to control the DVME-630. This offers a simple menu to control the DVME-630. No programming is required. Because of the modular design of the driver, its functions may be used through the menu shell or may be controlled by a user's program after rewriting the menu shell.

The Driver functions are:

- Install VME bus Interrupt Service Routine (ISR) to respond to DVME-630 buffer full flags. A small UNIX device driver is included.
- Initialize the VME bus interrupt system.
- Set the DVME-630 memory base address and test memory.
- Download the Exec, library and full local system to the DVME-630 DPR from a system binary file.
- Boot the local DVME-630 system and confirm.
- Allocate a VME bus Host buffer to receive DVME-630 data.
- Download a converted AFB file and start execution.
- Collect data to buffer or disk using swapped double buffer interrupts.
- Stop the AFB and save the DVME-630 data buffer to a file.
- Load and run a user COFF object file.
- Calibrate the A/D. Halt and reset the DSP. Quit to the OS.
- Auto run in batch mode (no menues).

VME bus Memory Map

Byte Address

15 8	7 0	
Not Used	Interrupt Vector ID (Read/Write)	Base+7FFFFh
Not Used	Command Register (Write Only)	Base+7FFFCh
Not Used		Base+7FFF8-Bh
Dual Port Random Access Memory		Base+7FFF7h (512kB)
		Base (DSP location 0)

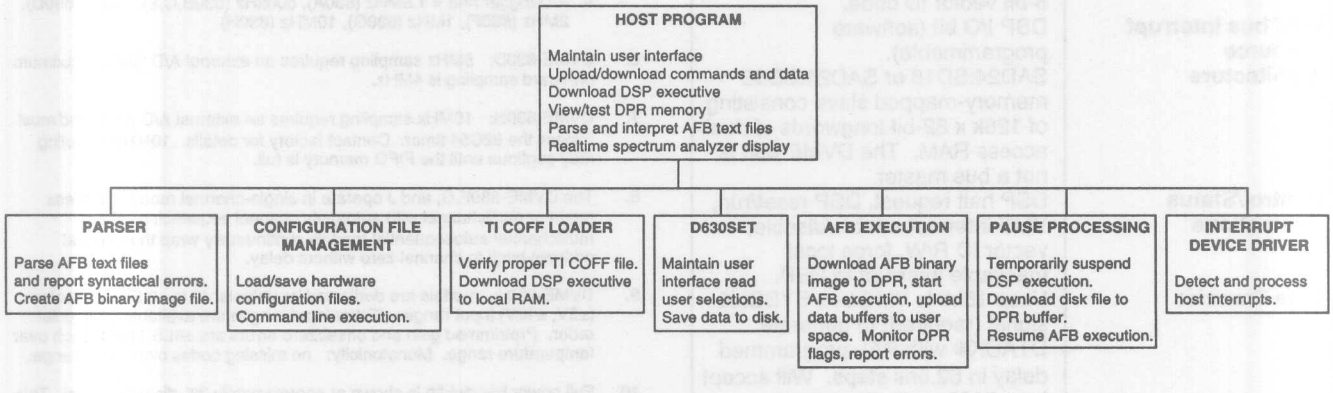


Figure 3. DVME-630EXEC Software

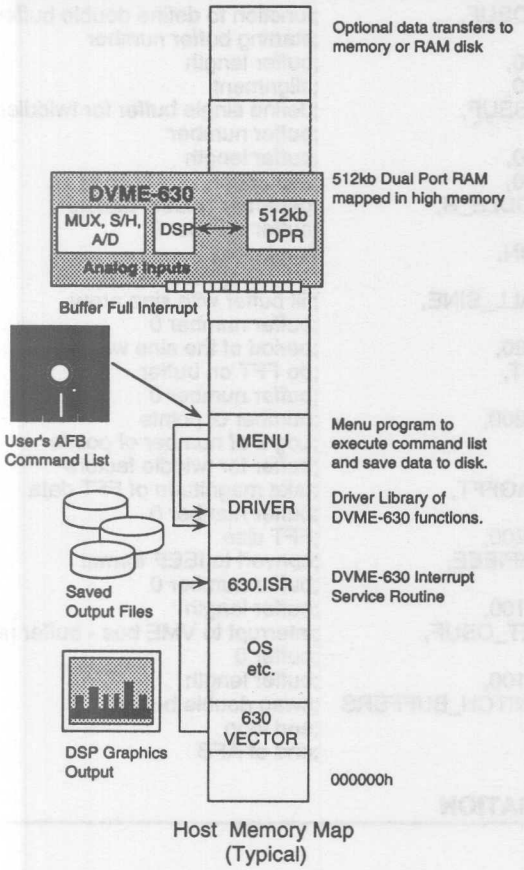


Figure 4. DVME-630 Host System Architecture

DSP Library Functions

Over 60 functions are included in the Executive AFB library. These are fully described in the DVME-630 User's manual (included with the board). The functions become resident when the scheduler is downloaded. Full commented source code to these functions is found in the DVME-630SRC package. Most functions are written in mix of high performance "C" and 320C30 Assembly language. Users may modify the functions or add their own functions and rebuild the system.

The AFB functions may be grouped into the following categories:

A/D Scan Routines

These functions initialize the A/D hardware for data acquisition - input channel addressing, 82C54 timer programming (sample count, sample rate), A/D triggering mechanisms, enable/disable local FIFO interrupts, enable/disable the A/D, reset the FIFO, local interrupt and DMA processing, and A/D calibration. A/D scan AFB's are typically called at the start of each AFB text file. Additional local hardware functions include PC-430DAC and PC-430DIG control.

Buffer Management Routines

Subroutines include local buffer allocation and maintenance - define single and double buffers, post buffer addresses to host area, sequence and swap double buffers during A/D collection loops, unravel large multi-channel buffers into individual buffers for each channel, high-speed data packing, data transfer between buffers, interrupt or post status bit to the host when data is ready for upload, maintain overlfow flags, declare MEM-30 sizes (1Mb, 4Mb), MEM-30 transfers, and pause DSP execution temporarily to allow host access to local buffers. Buffer allocation is done at the beginning of each AFB text file.

DSP Array Math Routines

Local DSP math processing subroutines - FIR/IIR filtering, convolution, Hamming/Hanning/rectangular/Blackman-Harris/raised cosine windowing, complex FFT, real FFT, twiddle factor generation, sine/cosine tables, FFT calculations, constant buffer fills, bit reversal, and pre-trigger ring buffer maintenance. Many of these functions can be used within one AFB loop for real time A/D data processing.

Array Conversion Routines

Convert data within local buffers to different formats - IEEE-754 to TMS320C30 format, TMS320C30 to IEEE-754 format, 32-bit integer to 320 floating point format, floating point 320 to 32-bit integer format, sign extend 16-bit integers to 32-bit format, doubleword matrix addition and multiplication, and array division by a constant. All DSP processing uses an internal 32-bit floating point format that is optimized for hardware speed.

Single Variable Transcendentals

Data math calculations including sine, cosine, tangent, inverse sine, inverse cosine, inverse tangent, square root, powers, exponential, natural logorithms, and base 10 logarithms. These functions are also available in the TI "C" compliler library with user-written code.

Software Hierarchy

The relationship between software in the VME bus host and in the DVME-630 is illustrated in this diagram. Control flows downward from the user's Application Function Block (AFB) and A/D data flows upward.

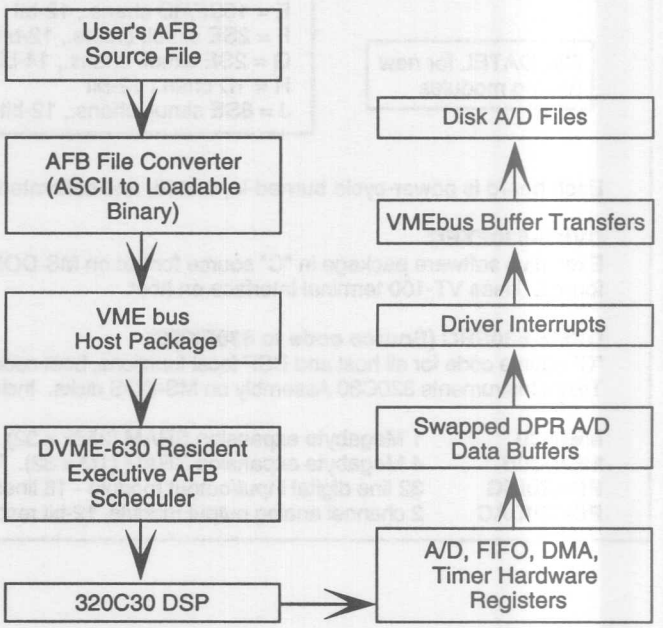


Figure 5. Software Hierarchy Flow Chart

Application Function Block (AFB) Programming

The DVME-630 system has been designed to optimize three competing objectives - easy-to-use, fast, powerful. To achieve these mutually exclusive goals, a high speed command list form of control is used. The Application Function Block (AFB) is a short list that calls local library functions. No local programming is needed. The user writes the AFB file with any text editor and it is then converted on the VME bus side to an internal binary form. The converted AFB is then downloaded to DVME-630 Dual Port RAM (DPR) and executed. The AFB is powerful because of full access to the local DSP library and because repeating functions may be looped. These loops in turn may be nested. Loops can run with a loop count or "forever" until stopped.

Unlike a slow ASCII interpreter, the AFB runs at the full speed of the 320C30 DSP with minimal overhead. And to accept fast A/D's without sample loss, only a fully integrated hardware/software system will handle the bandwidth. This hardware system consists of local FIFO A/D memory, local FIFO interrupts and a local Direct Memory Access (DMA) controller inside the DSP which runs in background. FIFO interrupts may cause DMA data block transfers while the DSP continues foreground processing.

Here is an AFB example which defines buffers, generates a sine wave, then prepares an FFT array for floating point output:

```
DEFDBUF,            ;function to define double buffer
0,                  ;starting buffer number
0x400,              ;buffer length
0x200,              ;alignment
DEFSBUF,            ;define single buffer for twiddles
2,                  ;buffer number
0x100,              ;buffer length
0x100,              ;alignment
TWIDDLE_R,          ;generate twiddle factors
2,                  ;buffer number 2
BEGIN,              ;begin flag
-1,                 ; -1 = loop forever flag
  CALL_SINE,        ;fill buffer with sine array
  0,                ;buffer number 0
  0x20,             ;period of the sine wave
  FFT,              ;do FFT on buffer
  0,                ;buffer number 0
  0x200,            ;number of points
  9,                ;Log 2 of number of points
  2,                ;buffer for twiddle factors
  MAGFFT,           ;take magnitude of FFT data
  0,                ;buffer number 0
  0x200,            ;FFT size
  DSPIEEE,          ;convert to IEEE format
  0,                ;buffer number 0
  0x100,            ;buffer length
  SET_OBUF,         ;interrupt to VME bus - buffer ready
  0,                ;buffer 0
  0x100,            ;buffer length
  SWITCH_BUFFERS    ;swap double buffers
END                 ;end loop
END                 ;end of AFB
```

ORDERING INFORMATION

DVME- ____ ____ ____ ____

CPU Speed

630 = 32MHz (standard)
630/40 = 40MHz (special order)

Call DATEL for new analog modules

A/D Type, Channels, Resolution

A = 4SE simul. chans., 12-bit
B = 4SE chans., 14-bit
C = 4SE chans., 12-bit
D = 1 D chan., 12-bit
E = 16SE/8D chans., 12-bit
F = 2SE simul. chans., 12-bit
G = 2SE simul. chans., 14-bit
H = 1D chan., 12-bit
J = 8SE simul. chans., 12-bit

FIFO Memory Size

1 = 1024 A/D samples
2 = 4096 A/D samples

Input Polarity

A = Bipolar
B = Unipolar
Use this designator *only* for G and J models requiring polarity selection.

Example: DVME-630J2A
8 simultaneous A/D's, 4k FIFO, ±5V input, 32MHz CPU.

Each board is power-cycle burned-in, tested, and calibrated. All models include a user's manual. One year warranty.

DVME-630EXEC
Executive software package in "C" source format on MS-DOS disks. Includes all local functions in downloadable binary format. Uses VT-100 terminal interface on host.

DVME-630SRC (Source code to 630EXEC)
"C" source code for all host and DSP local functions, boot code, vectors, scheduler, DSP math library, etc. Supplied in "C" and Texas Instruments 320C30 Assembly on MS-DOS disks. Includes UNIX device driver and UM-CMDRSRC User Manual.

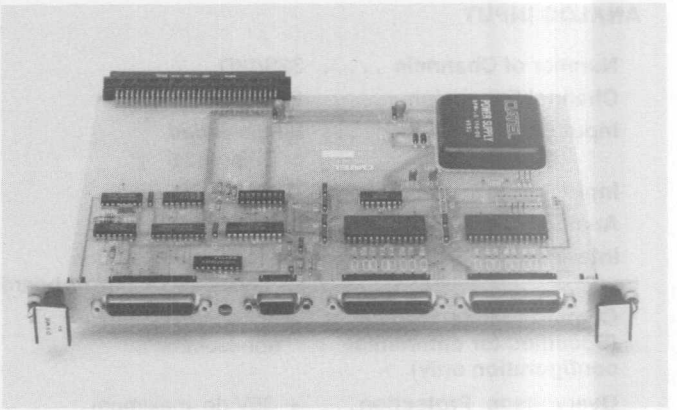
MEM-30	1 Megabyte expansion SRAM (256k x 32). Total installed capacity is 1.5Mb. See MEM-30 data sheet.
MEM-30B	4 Megabyte expansion SRAM (1M x 32). Total usable capacity is 4.5Mb. See MEM-30 data sheet.
PC-430DIG	32 line digital input/output module - 16 lines in, 16 lines out. See PC-430DIG/PC-430DAC data sheet.
PC-430DAC	2 channel analog output module, 12-bit resolution, 10µs settling. See PC-430DIG/PC-430DAC data sheet.

DATEL®
INNOVATION and EXCELLENCE

DVME-641
32-Channel, High-Level VMEbus Expansion Board

FEATURES

- Accepts 32 single-ended/16 differential expansion channels
- Directly accepts high-level inputs
- Hardware compatible with VMEbus specifications
- Interfaces to DATEL's DVME-601/611/612 A/D boards
- 6 Microseconds settling time
- 0.01% Full-scale range accuracy
- Low-cost
- Cascadable to up to 256 channels
- Includes a board selection LED lamp



The DVME-641 offers channel expansion to DATEL's DVME-601/611/612 Series of A/D boards. The channel expansion board is designed to accept high-level inputs from up to 32 single-ended or 16 differential input channels. The DVME-641 draws power from the VMEbus P1 connector and fits into VMEbus card cages.

GENERAL DESCRIPTION

The DVME-641 is a low-cost channel expansion board that interfaces directly to DATEL's DVME-601/611/612 high-performance A/D boards. The board externally multiplexes up to 32 single-ended or 16 differential high-level input channels. The channel expansion board fits into a typical VMEbus host system. The DVME-641 is specifically useful for applications involving multiple-channel data acquisition or controlling numerous discrete process control loops. The low cost per channel makes the board ideal for most applications.

Figure 1 shows a typical multi-channel application for data acquisition from different types of inputs. In this application the host system selects the expansion channel on the DVME-641, DVME-643 or DVME-645 through the DVME-601/611/612 A/D board. The DVME-601/611/612 digital data is available on the VMEbus data lines for host system access.

ORDERING INFORMATION

DVME-641	32S/16D MUX board

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).

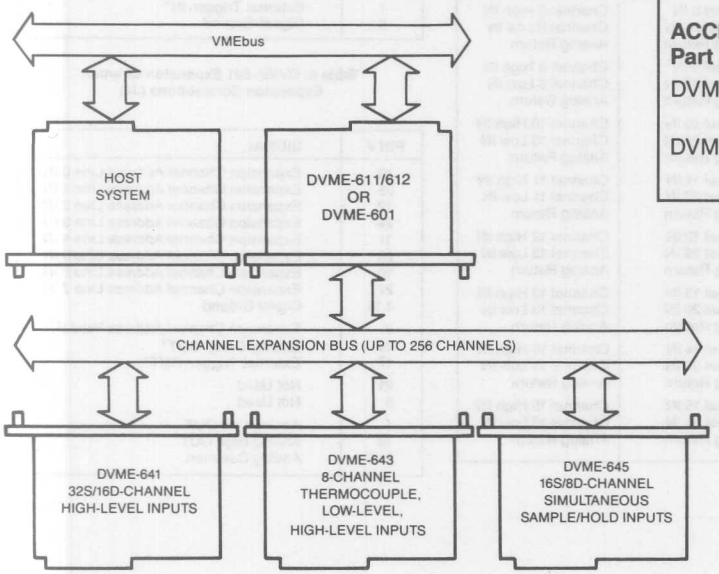


Figure 1: DVME-641 Application Configuration

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C unless otherwise noted)

ANALOG INPUT

Number of Channels	32S/16D
Channel Expansion	256S/256D*
Input Configuration	Single-ended or Differential
Input Range	± 10V dc
Analog Output	Differential
Interface	Analog Expansion Bus for DVME-601/611/612 boards
Common Mode Voltage (Specified for differential configuration only)	±10V dc, maximum non-isolated
Overvoltage Protection	± 35V dc, maximum
Off-Channel Leakage current	0.03 nanoamperes, typical 60 nanoamperes, maximum
On-Channel Leakage Current	0.1 nanoamperes,typical 300 nanoamperes, maximum
Output Settling Time (0 to 10V step input, channel-to-channel settling)	6 μseconds, maximum to rated accuracy
Full-scale Range Accuracy	0.01%, maximum
Output Impedance	2.5 Kohms, maximum

*Up to 10 slave MUX boards may be driven from one A/D master board at derated settling.

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector	96-pin male DIN connector
Analog Input - J1,J2 Connectors	Two 25-pin D-type DB-25S female connectors
External Trigger - J3 Connector	9-pin D-type DB-9S female connector
Analog Expansion - J4 Connector	25-pin D-type DB-25S female connector

POWER SUPPLY REQUIRMENTS

+5V dc ±0.5% at 0.4A typical, 0.6A maximum from P1 VMEbus connector

PHYSICAL CHARACTERISTICS

Outline Dimensions	9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)
Weight	11 oz. (311.85 grams)
Operating Temperature Range	0 to +60 °C
Storage Temperature Range	-20 to +80 °C
Relative Humidity	0 to 90% non-condensing

I/O CONNECTIONS

The DVME-641 uses J1, J2, J3, and J4 for analog input, external trigger, and channels expansion connections. Tables 1,2, 3, and 4 list these signals. VMEbus IACK and bus grant signals are daisy-chained.

Table 1: DVME-641 Analog Input Connector (J1)

PIN #	Single-ended	Differential
24	Channel 0 IN	Channel 0 High IN
12	Channel 16 IN	Channel 0 Low IN
25	Analog Return	Analog Return
10	Channel 1 IN	Channel 1 High IN
23	Channel 17 IN	Channel 1 Low IN
11	Analog Return	Analog Return
21	Channel 2 IN	Channel 2 High IN
9	Channel 18 IN	Channel 2 Low IN
22	Analog Return	Analog Return
7	Channel 3 IN	Channel 3 High IN
20	Channel 19 IN	Channel 3 Low IN
8	Analog Return	Analog Return
18	Channel 4 IN	Channel 4 High IN
6	Channel 20 IN	Channel 4 Low IN
19	Analog Return	Analog Return
4	Channel 5 IN	Channel 5 High IN
17	Channel 21 IN	Channel 5 Low IN
5	Analog Return	Analog Return
15	Channel 6 IN	Channel 6 High IN
3	Channel 22 IN	Channel 6 Low IN
16	Analog Return	Analog Return
1	Channel 7 IN	Channel 7 High IN
14	Channel 23 IN	Channel 7 Low IN
2	Analog Return	Analog Return

Table 2: DVME-641 Analog Input Connector (J2)

PIN #	Single-ended	Differential
24	Channel 8 IN	Channel 8 High IN
12	Channel 24 IN	Channel 8 Low IN
25	Analog Return	Analog Return
10	Channel 9 IN	Channel 9 High IN
23	Channel 25 IN	Channel 9 Low IN
11	Analog Return	Analog Return
21	Channel 10 IN	Channel 10 High IN
9	Channel 26 IN	Channel 10 Low IN
22	Analog Return	Analog Return
7	Channel 11 IN	Channel 11 High IN
20	Channel 27 IN	Channel 11 Low IN
8	Analog Return	Analog Return
18	Channel 12 IN	Channel 12 High IN
6	Channel 28 IN	Channel 12 Low IN
19	Analog Return	Analog Return
4	Channel 13 IN	Channel 13 High IN
17	Channel 29 IN	Channel 13 Low IN
5	Analog Return	Analog Return
15	Channel 14 IN	Channel 14 High IN
3	Channel 30 IN	Channel 14 Low IN
16	Analog Return	Analog Return
1	Channel 15 IN	Channel 15 High IN
14	Channel 31 IN	Channel 15 Low IN
2	Analog Return	Analog Return

Table 3: DVME-641 External Trigger Input Connections (J3)

PIN #	SIGNAL
1	External Trigger IN*
6	Digital Ground

Table 4: DVME-641 Expansion Channel Expansion Connections (J4)

PIN #	SIGNAL
13	Expansion Channel Address Line 0 IN
25	Expansion Channel Address Line 1 IN
12	Expansion Channel Address Line 2 IN
24	Expansion Channel Address Line 3 IN
11	Expansion Channel Address Line 4 IN
23	Expansion Channel Address Line 5 IN
10	Expansion Channel Address Line 6 IN
22	Expansion Channel Address Line 7 IN
4,16	Digital Ground
9	Expansion Channel Address Valid IN
20	Setting Delay OUT*
17	External Trigger OUT*
21	Not Used
5	Not Used
1	Analog Low OUT
14	Analog High OUT
2,15	Analog Common

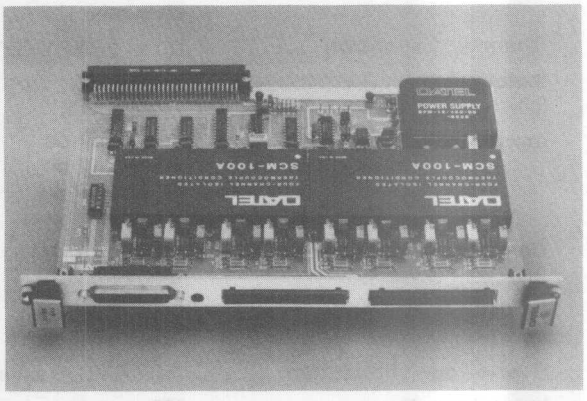
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DVME-643
8-Channel, Isolated Analog VMEbus Expansion Board

FEATURES

- **Offers channel expansion to DATEL's DVME-601/611/612 A/D boards**
- **Two models of channel expansion boards**
  DVME-643T: Thermocouple and low-level inputs
  DVME-643H: High-level inputs
- **On-board cold junction compensation sensor**
- **Offers 1000V peak isolation**
- **On-board signal conditioning**
- **120 dB minimum CMRR**
- **55 dB minimum NMR**
- **2.5 millisecond settling time**
- **On-board dc-to-dc power converter**
- **Cascadable to up to 10 MUX boards**
- **Includes a board selection LED lamp**



The DVME-643 boards offer channel expansion to DATEL's DVME-601/611/612 A/D boards. These multiplexer boards provide 1000V isolation and signal conditioning for eight thermocouple, low-level, or high-level inputs. The DVME-643T board incorporates a cold junction compensation output for thermocouple inputs to correct against reference junction temperature variations.

GENERAL DESCRIPTION

Designed specifically for applications requiring multiple channel data acquisition, the DVME-643 boards expand the analog input capability of DATEL's DVME-601/611/612 A/D boards. The DVME-643 boards are offered in two versions. The DVME-643T provides isolation and signal conditioning for thermocouple and low-level inputs. The DVME-643H accepts for high-level voltage and 4-to-20 mA current loop inputs.

The DVME-643T allows mixing thermocouple and low-level signals on the same board. The DVME-601/611/612 boards offer channel expansion for up to 256 channels. In addition to the DVME-643 boards, DATEL's channel expansion boards for high-level and simultaneous sample and hold inputs may also be used with a DVME-601/611/612 board. Figure 1 shows typical multi-channel application configuration.

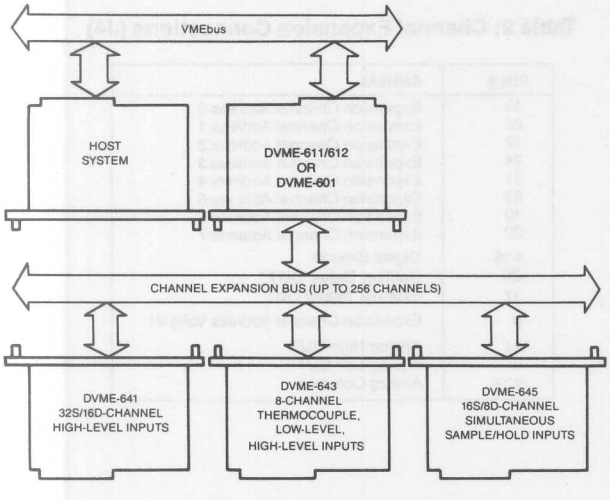


Figure 1: DVME-643 Application Configuration

ORDERING INFORMATION

DVME-643

- T — Thermocouple and low-level isolated inputs
  input ranges: ±25.6, 51.2, and 102.4mV
- H — High-level voltage and current loop isolated inputs
  High-level voltage ranges: ±5V dc
  Current loop inputs: 4-to-20 mA

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).
8158760	12-pin connector (included)

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, unless otherwise noted)

ANALOG INPUT

Number of Channels . . . . . 8 Differential and CJC channels

Channel Expansion . . . . . Up to 256S/256D*

Isolation . . . . . 750V RMS
(ch-ch. & ch.-bus) 1000V Peak

Input Range DVME-643T . . . . . ±25.6 mV dc
±51.2 mV dc
±102.4 mV dc

DVME-643H . . . . . ±5V dc

Common Mode Voltage . . . . . 750V RMS
AC, 50 or 60Hz 1000V Peak

Input Bias Current . . . . . 8 nano amperes, maximum

Overvoltage Protection . . . . . 130V RMS, maximum

Input Impedance, differential input to ground . . . . . 100 megohms

Common Mode Rejection Ratio, f = .01 to 100Hz
DVME-643T . . . . . 120 dB, minimum
DVME-643H . . . . . 110 dB, minimum

Normal Mode Rejection . . . . . 55 dB, minimum
50 or 60 Hz

Settling Time . . . . . 2.5 milliseconds, maximum

dc Gain Accuracy
DVME-643T . . . . . 0.03% FSR, minimum
DVME-643H . . . . . 0.05% FSR, minimum

Gain Drift . . . . . 35 ppm/°C, maximum

Offset Drift
DVME-643T . . . . . 3 μV/°C, maximum
DVME-643H . . . . . 60 μV/°C, maximum

CJC Error
At Room Temperature . . . . . 0.5°C, maximum
At Full Temperature Range . . . 1.5°C, maximum

Output Impedance . . . . . 0.5 K ohms, maximum

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1A typical, 1.5A maximum from P1 VMEbus connector.

I/O CONNECTIONS

The DVME-643 uses J1 and J2 for analog input connections and J4 for channel expansion connections. Tables 1 and 2 list these signals. VMEbus IACK and bus grant signals are daisy-chained.

CONNECTOR SPECIFICATIONS

VMEbus-P1 Connector . . . . . 96-pin male DIN connector

Analog Input J1 and J2 Connectors . . . . . 12-pin male connector

Analog Expansion J4 Connector . . . . . 25-pin D-type female connector, DB-25S

PHYSICAL—ENVIRONMENTAL

Outline Dimensions . . . . . 9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)

Weight . . . . . 1 lb (453.59 grams)

Operating Temperature Range . . 0 to +60°C

Storage Temperature Range . . . . . -20 to +80°C

Relative Humidity . . . . . 0 to 90%, non-condensing

*Up to 10 slave MUX boards may be driven from one A/D master board.

Table 1: Analog Input Connections (J1 and J2)

PIN #	SIGNAL (J1)
12	Channel 0 High IN
11	Channel 0 Low IN
10	Analog Return
9	Channel 1 High IN
8	Channel 1 Low IN
7	Analog Return
6	Channel 2 High IN
5	Channel 2 Low IN
4	Analog Return
3	Channel 3 High IN
2	Channel 3 Low IN
1	Analog Return

PIN #	SIGNAL (J2)
12	Channel 4 High IN
11	Channel 4 Low IN
10	Analog Return
9	Channel 5 High IN
8	Channel 5 Low IN
7	Analog Return
6	Channel 6 High IN
5	Channel 6 Low IN
4	Analog Return
3	Channel 7 High IN
2	Channel 7 Low IN
1	Analog Return

Table 2: Channel Expansion Connections (J4)

PIN #	SIGNAL
13	Expansion Channel Address 0
25	Expansion Channel Address 1
12	Expansion Channel Address 2
24	Expansion Channel Address 3
11	Expansion Channel Address 4
23	Expansion Channel Address 5
10	Expansion Channel Address 6
22	Expansion Channel Address 7
4,16	Digital Ground
20	Settling Delay OUT*
17	External Trigger OUT
9	Expansion Channel Address Valid IN
14	Analog High OUT
1	Analog Low OUT
2,15	Analog Common

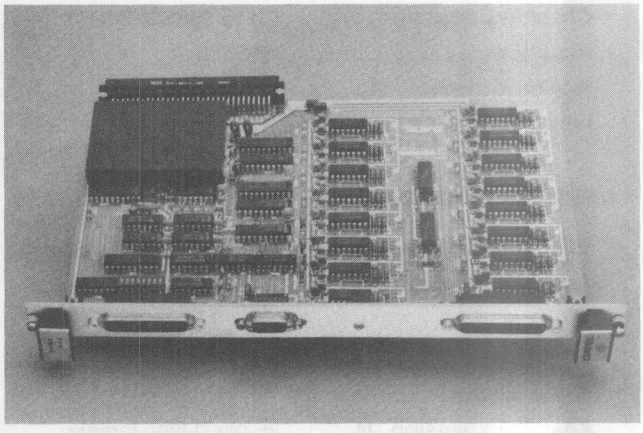
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DVME-645
16-Channel, Simultaneous S/H VMEbus Expansion Board

FEATURES

- **Offers channel expansion to DVME-601/611/612 A/D boards**
- **Offers simultaneous sample-and-hold capability to up to 16S/8D channels**
- **1.2 μV/μS sample-and-hold droop rate**
- **6 Microsecond settling time**
- **Complete compatibility to VMEbus hardware specifications**
- **Cascadable to up to 256 channels**
- **0.05% Full-scale range accuracy**
- **On-board dc-to-dc converter**



The DVME-645 is designed to provide channel expansion to DATEL's DVME-601/611/612 boards for applications requiring sample and hold capability. The board is equipped with 16 sample and hold amplifiers, acquiring data simultaneously from 16 channels. The board is ideally suited for transient analysis, signal reconstruction and related applications.

GENERAL DESCRIPTION

The DVME-645 offers simultaneous sample-and-hold capability to DATEL's family of multiplexer boards. The board expands the analog input channels of the DVME-601/611/612 A/D boards. In a typical application, the DVME-645 is usable with other multiplexer boards using thermocouple, isolated and non-isolated voltage inputs. Figure 1 shows the channel expansion to the DVME-601/611/612 A/D boards.

Simultaneous Sample-and-Hold

A sample-and-hold circuit holds or freezes a changing analog input signal for up to a few milliseconds. With 16 on-board amplifiers, the DVME-645 simultaneously holds analog signals from 16 individual channels. An A/D subsystem (DVME-601/611/612) may scan and convert the samples stored. The digital data now represents the analog signal values at an instant of time from all the 16 channels.

The DVME-645 also allows measuring high-speed transients and spikes during a specified window of time. For applications requiring sampling at rates up to 8 MHz all 16 channels may be connected to a single measuring point. The sample-and-hold circuits may then sequentially acquire the analog input signal. In this application, the DVME-645 functions as a very low-cost 8 MHz storage device. Typical applications of the DVME-645 with the DVME-601/611/612 include pulse analysis and reconstruction and data skew elimination for seismic measurements.

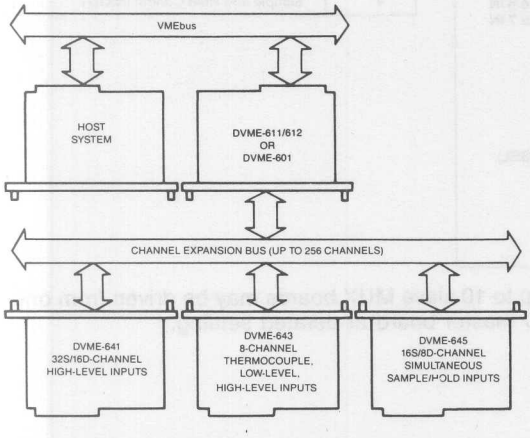


Figure 1: DVME-645 Application Configuration

ORDERING INFORMATION

DVME-645	16S/8D SSH MUX board

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, unless otherwise noted)

Number of Channels . . . . . 16S/8D non-isolated

Channel Expansion . . . . . Up to 256S/256D*

Input Range . . . . . ±10V dc

Analog Output . . . . . Differential

Interface . . . . . Analog expansion bus for DVME-611/612/601 boards

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector . . . . 96-pin male DIN connector

Analog Input J1 Connector 25-pin D-type female connector

External Trigger and Sample-and-hold Control J3 Connector . . . . . 9-pin D-type female connector

Analog Expansion J4 Connector . . . . . 25-pin D-type female connector

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 2.0A typical, 3.0A maximum from P1 VMEbus connector.

I/O CONNECTIONS

The DVME-645 uses J1 and J4 connectors for analog input and channel expansion connections respectively. Tables 1 and 2 list the signals for the connections. Table 3 lists signals for trigger and sample-and-hold control. VMEbus IACK and bus grant signals are daisy-chained.

LED front panel lamp . . . . . lights when board is addressed

ANALOG SPECIFICATIONS

Common Mode Voltage . . . . ±10V dc, maximum

Over Voltage Protection . . . ±35V dc, maximum

Input Bias Current . . . . . 300 nanoamperes, maximum

Input Impedance . . . . . 1 Megohm, minimum

Output Settling Time (For 0 to -10V step input, channel-to-channel settling) . . . . . 6 μseconds, maximum to rated accuracy

dc Gain Accuracy . . . . . 0.05%, minimum

Output Impedance . . . . . 0.5 Kohms, maximum

Input Offset Voltage . . . . . 1.0 mV, maximum

Input Offset Voltage Drift . . . . . 20 μV/°C, maximum

Aperture Delay . . . . . 50 nS

Aperture Time . . . . . 100 nS

Sample-and-Hold Droop Rate . . . 1.2 μV/μS, typical
2.0 μV/μS, maximum

Sample-and-Hold Pedestal . 1.0 mV, typical
2.5 mV, maximum

PHYSICAL—ENVIRONMENTAL

Outline Dimensions . . . . . 9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)

Weight . . . . . 12.5 Oz. (354.75 grams)

Operating Temperature Range . . . . 0 to +60°C

Storage Temperature Range . . . . . 20 to +80°C

Relative Humidity . . . . . 0 to 90% non-condensing

Table 1: DVME-645 Analog Input Connector (J1)

PIN #	Single-ended	Differential
24	Channel 0 IN	Channel 0 High IN
12	Channel 8 IN	Channel 0 Low IN
25	Analog Return	Analog Return
10	Channel 1 IN	Channel 1 High IN
23	Channel 9 IN	Channel 1 Low IN
11	Analog Return	Analog Return
21	Channel 2 IN	Channel 2 High IN
9	Channel 10 IN	Channel 2 Low IN
22	Analog Return	Analog Return
7	Channel 3 IN	Channel 3 High IN
20	Channel 11 'N	Channel 3 Low IN
8	Analog Return	Analog Return
18	Channel 4 IN	Channel 4 High IN
6	Channel 12 IN	Channel 4 Low IN
19	Analog Return	Analog Return
4	Channel 5 IN	Channel 5 High IN
17	Channel 13 IN	Channel 5 Low IN
5	Analog Return	Analog Return
15	Channel 6 IN	Channel 6 High IN
3	Channel 14 IN	Channel 6 Low IN
16	Analog Return	Analog Return
1	Channel 7 IN	Channel 7 High IN
14	Channel 15 IN	Channel 7 Low IN
2	Analog Return	Analog Return

Table 2: DVME-645 Expansion Connections (J4)

PIN #	SIGNAL
13	Expansion Channel Address Line 0 IN
25	Expansion Channel Address Line 1 IN
12	Expansion Channel Address Line 2 IN
24	Expansion Channel Address Line 3 IN
11	Expansion Channel Address Line 4 IN
23	Expansion Channel Address Line 5 IN
10	Expansion Channel Address Line 6 IN
22	Expansion Channel Address Line 7 IN
4,16	Digital Ground
9	Channel Address Valid IN
8	Start Conversion Strobe IN
20	Strobe Delay OUT*
7	End of Conversion IN
19	End of Scan IN
17	External Trigger OUT*
6	General Purpose Input (XMODSEL)
5,21	Not Used
1	Analog Low OUT
14	Analog High OUT
2,15	Analog Common

Table 3: DVME-645 Digital Control Connections (J3)

PIN #	SIGNAL
1	External Trigger IN*
6	Digital Ground
9	Sample/Hold Skew IN
5	Sample/Hold Skew OUT
3	Sample and Hold Skew Clock IN/OUT
4	Sample and Hold Control IN/OUT

*Up to 10 slave MUX boards may be driven from one A/D master board at derated settling.

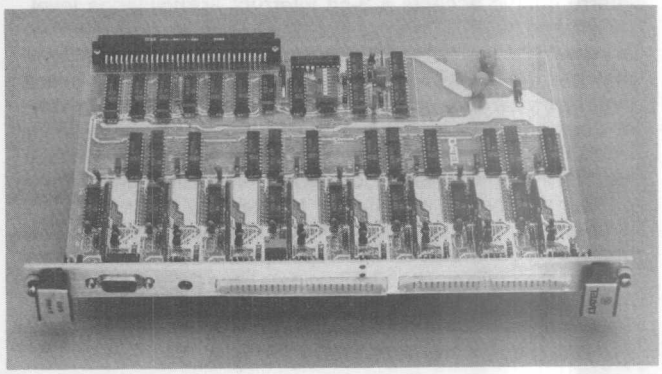
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DATEL®
INNOVATION and EXCELLENCE

DVME-660
48-Line, Digital I/O VMEbus Board

FEATURES

- Complete compatibility with VMEbus specifications
- 48 Digital I/O lines
- Software programmable input and outputs
- Interrupt levels, IRQ1 through IRQ7
- On-board timer
- 24- and 16-stage timer operation
- Interrupts on 1. Timer
  2. Compare register
  3. External trigger
- Compatible with GORDOS I/O module systems
- Compatible with OPTO-22 I/O module systems (PB-24 or PB-16)



DATEL expands its VMEbus product line with the DVME-660. The DVME-660 has 48 individually programmable TTL input or output lines. The on-board hardware includes an interrupt controller that allows up to seven user-programmable interrupt lines and a timer that allows delays up to a few minutes.

GENERAL DESCRIPTION

The DVME-660 is a high-performance digital I/O board that allows programming 48 lines individually. The board is electrically and mechanically compatible with GORDOS and OPTO-22 I/O module systems. The board is ideally suitable for industrial and process control applications.

Functionally the board consists of six bi-directional ports of eight lines each, a programmable timer and a VMEbus interrupter. The data direction of the eight lines in each port is programmable by the host system. The timer may receive the input frequency from the VMEbus SYSCLK signal or an on-board RC network. 16 of 24 timer stages are programmable by the VMEbus data lines. The timer is also programmable to bypass the first eight stages. Figure 1 shows the DVME-660 functional block diagram.

ORDERING INFORMATION

DVME-660 Includes user manual.

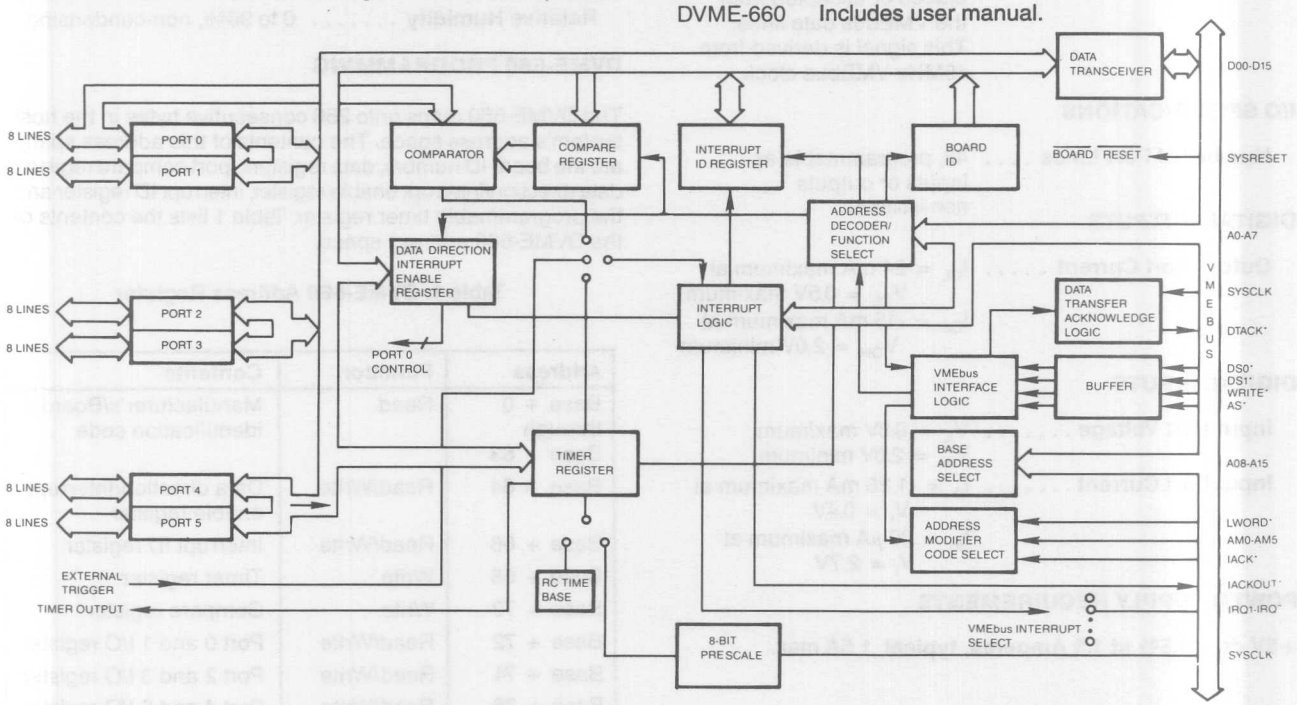


Figure 1: DVME-660 Functional Block Diagram

If enabled, the DVME-660 interrupt logic section generates an interrupt request on one of the VMEbus interrupt lines (IRQ1* through IRQ7*). The interrupt line is jumper-selectable. The interrupt logic accepts a 3-bit interrupt acknowledge level, IACK*, and IACKIN* signals from the host system as interrupt acknowledge and daisy chain input signals. If this interrupt level matches the DVME-660 interrupt request level, the on-board logic loads the interrupt ID number on to the VMEbus. If the level does not match, the board generates the daisy chain IACKOUT* signal. The DVME-660 may generate interrupt request from one of three sources: timer section, port 0 comparator section, or an external trigger. The timer output is jumper-selectable to cause periodic VMEbus interrupts. The board also generates an interrupt if port 0 inputs match data in compare register. The VMEbus data lines (D00 through D07) may load the compare register.

FUNCTIONAL SPECIFICATIONS

(Typical at 25 °C, unless otherwise noted)

INTERFACE SPECIFICATIONS

Data Bus	16 bits (A16:D16 slave)
Address Bus	Short I/O space, 16 address lines, 6 address modifier lines. Uses address modifier codes 29H, 2DH, 39H and 3DH
Interrupts	IRQ1* through IRQ7*
Memory Mapping	Short I/O space, user or supervisor, 256 words allocated per board
Data Transfer	DTACK* signal line. Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines. This signal is derived from 16MHz VMEbus clock

I/O SPECIFICATIONS

Number of Port Lines	48, programmable as inputs or outputs non-isolated

DIGITAL OUTPUTS

Output Port Current	I_{OL} = 24 mA maximum at V_{OL} = 0.5V maximum I_{OH} = -15 mA maximum at V_{OH} = 2.0V minimum

DIGITAL INPUTS

Input Port Voltage	V_{IL} = 0.8V maximum V_{IH} = 2.0V minimum
Input Port Current	I_{IL} = -1.26 mA maximum at V_i = 0.4V I_{IH} = 20 μA maximum at V_i = 2.7V

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1.3 Amperes, typical ,1.5A max.

VMEbus Interface

The DVME-660 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data input and output purposes. The DVME-660 generates the data acknowledge (DTACK*) signal to notify acceptance of data from the VMEbus data lines, D00 through D15. The DTACK* signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes VMEbus control lines (WRITE*, DS0*, DS1*, and SYSRESET*) to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-660 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector	96-pin male connector
Port Connectors J1 and J2	50-pin header male flat cable, 0.050" ctrs dual row
Trigger Control Connector J3	9-pin D-type female connector, DS-9S

PHYSICAL CHARACTERISTICS

Outline Dimensions	9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)
Weight	1 lb (453.6 grams)
Operating Temperature Range	0 to +60 °C
Storage Temperature Range	-20 to +80 °C
Relative Humidity	0 to 90%, non-condensing

DVME-660 PROGRAMMING

The DVME-660 maps onto 256 consecutive bytes in the host system's address space. The contents of this address space are the board ID number, data registers, port compare register, data direction/interrupt enable register, interrupt ID register and the programmable timer register. Table 1 lists the contents of the DVME-660 address space.

Table 1: DVME-660 Address Register

Address	Function	Contents
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 64	Read/Write	Data direction/Interrupt enable register
Base + 66	Read/Write	Interrupt ID register
Base + 68	Write	Timer register
Base + 70	Write	Compare register
Base + 72	Read/Write	Port 0 and 1 I/O register
Base + 74	Read/Write	Port 2 and 3 I/O register
Base + 76	Read/Write	Port 4 and 5 I/O register

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Data Direction/Interrupt Enable Register

The host system may program bits 0 through 5 of this register to assign direction of the six I/O ports. When programmed, all eight lines in a port will function as either inputs or outputs. Programming the bit 6 of this register enables the on-board interrupt logic. If this bit is set, the DVME-660 interrupts the host system. The interrupt may be from the timer section, the port 0 comparator section, or an external trigger. Figure 2 shows the format of this register.

Word address: Base + 64

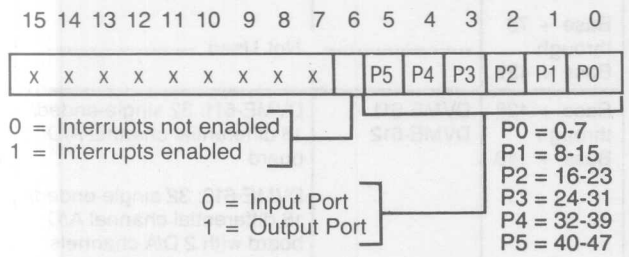


Figure 2: DVME-660 Data Direction/Interrupt Enable Register

Interrupt ID Register

This register contains the user-loaded interrupt ID number. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK* and the daisy chain IACKIN* signal lines. If the DVME-660 interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number onto the VMEbus (low byte). Figure 3 shows the format of the interrupt ID register.

Word address: Base + 66

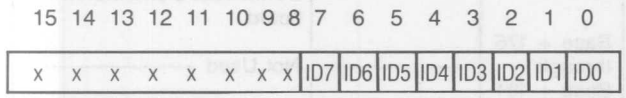


Figure 3: DVME-660 Interrupt ID Register Format

Port Compare Register

The DVME-660 has a port comparator section that compares inputs from port 0 to the contents of the port compare register. The host system may load the port compare register using VMEbus data lines D00 through D07. The port comparator section generates a single VMEbus interrupt if the port 0 inputs match the port compare register contents. Figure 4 shows the format of the port compare register.

Word address: Base + 70

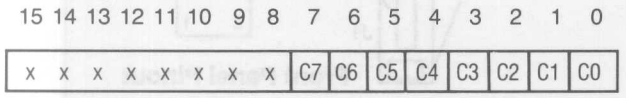


Figure 4: DVME-660 Port Compare Register

Programmable Timer Register

Eight LSB's of this register allows programming the on-board programmable timer section. Bits 0 through 3 assign a timer divide ratio that selects one of sixteen timer stages. The maximum timer input frequency is approximately 1MHz. Bit 4 sets the time for 24 or 16-stage operation by bypassing the first eight stages. Programming bit 6 enables the port 0 comparator. Bit 7 is usable to turn ON an on-board LED lamp. Figure 5 shows the format of this register. Timer: MC14536.

Word address: Base + 68

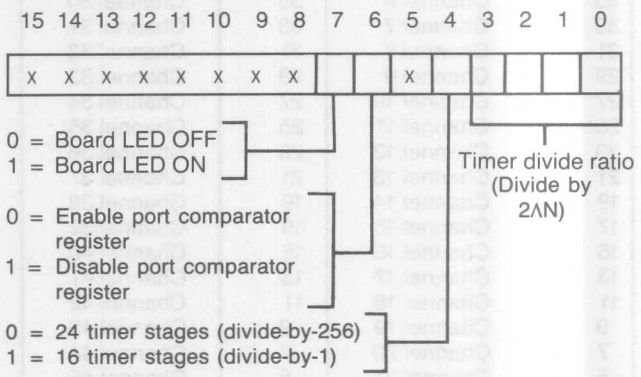


Figure 5: DVME-660 Programmable Timer Register

Port I/O Registers

The DVME-660 uses three 16-bit registers as six 8-line ports. The lower 8 bits of these registers correspond to ports 0, 2, and 4 respectively and the higher 8 bits correspond to ports 1, 3, and 5 respectively. Figure 6 shows the format of these registers.

Word address: Base + 72, 74 and 76

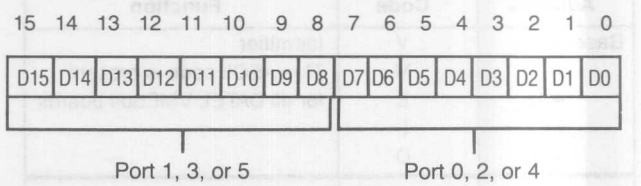


Figure 6: DVME-660 Port I/O Registers

Note: All data is inverted.

I/O CONNECTIONS

The DVME-660 digital I/O board uses J3 connection for trigger control, and J1 and J2 connectors for digital I/O connections. Tables 2 and 3 lists signals for these connectors.

Table 2: Trigger Control Connections (J3)

Pin #	Signal
1	External Interrupt Request In
2	Trigger Output
3	External Timer Clock In
4	No Connection
5,6	+5V dc
7,8,9	Digital Ground

Table 3: DVME-660 I/O Connections (J1 and J2)

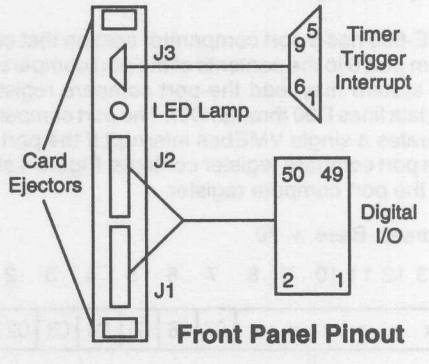
J1 Connector		J2 Connector	
Pin #	Signal	Pin #	Signal
47	Channel 0	47	Channel 24
45	Channel 1	45	Channel 25
43	Channel 2	43	Channel 26
41	Channel 3	41	Channel 27
39	Channel 4	39	Channel 28
37	Channel 5	37	Channel 29
35	Channel 6	35	Channel 30
33	Channel 7	33	Channel 31
31	Channel 8	31	Channel 32
29	Channel 9	29	Channel 33
27	Channel 10	27	Channel 34
25	Channel 11	25	Channel 35
23	Channel 12	23	Channel 36
21	Channel 13	21	Channel 37
19	Channel 14	19	Channel 38
17	Channel 15	19	Channel 39
15	Channel 16	15	Channel 40
13	Channel 17	13	Channel 41
11	Channel 18	11	Channel 42
9	Channel 19	9	Channel 43
7	Channel 20	7	Channel 44
5	Channel 21	5	Channel 45
3	Channel 22	3	Channel 46
1	Channel 23	1	Channel 47
49	+5V dc OUT	49	+5V dc OUT
2 through 50	Digital Ground	2 through 50	Digital Ground

DVME-660 Board Identification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	6	
+ 1F	0	

DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------



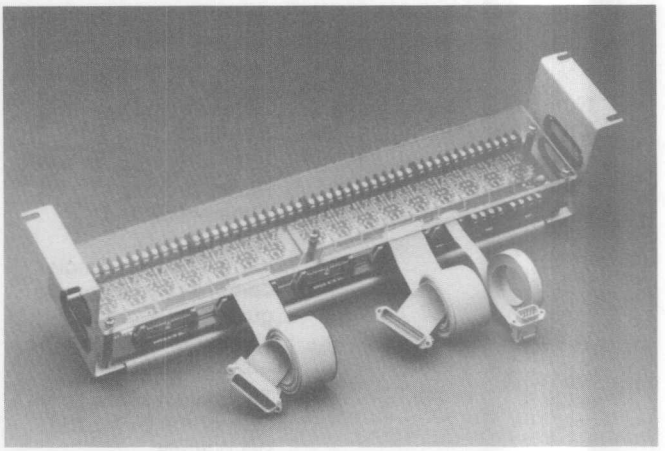
Front Panel Pinout

DATEL®
INNOVATION and EXCELLENCE

DVME-691A/D
Rack-mounted, Signal-Conditioning Screw Terminator Panel

FEATURES

- **Rack-mounted screw-terminations for factory wiring**
- **Two models available:**
  DVME-691A for analog inputs
  DVME-691D for analog outputs
- **Both versions have component etch wiring ready to accept discrete components for signal conditioning**
- **DVME-691A Version includes component pads for shunts, attenuators, filters, and spike clamps**
- **DVME-691D Version includes component pads for current loop excitation**
- **DVME-691A handles up to 32 single-ended inputs**
- **DVME-691D provides up to eight analog output channels**
- **Designed for 19 inch RETMA racks**
- **Complete with mounting hardware and cables**
- **Plexiglas safety shield for connector labeling**



The DVME-691A and DVME-691D termination panels offer a convenient way of interfacing field wiring to DATEL's line of VMEbus boards. In addition, the panels are designed to incorporate discrete signal conditioning components for either analog inputs or outputs.

GENERAL DESCRIPTION

Offering a convenient method of connecting A/D or D/A channel wiring through screw terminators, the DVME-691 rack-mount interface panel is ideal for industrial and process control analog I/O connections. Field cabling need no longer be brought directly to the I/O connectors of the VMEbus boards. Instead, the user terminates all field wiring at the panel then uses DATEL's ribbon cabling system to bring signals to the specific boards.

The 3.5-inch high panel mounts into a standard RETMA 19" rack, letting the unit mount directly in the same rack as the user's VMEbus cardcage. All interwiring consists of flat ribbon cables, affording a quick disconnect capability.

Both versions interface I/O channels of DATEL's VMEbus boards to the user's field wiring using dedicated connectors, signal paths, and additional etch for user-installed discrete components. The DVME-691A can accommodate up to 32 single-ended or 16 differential analog input channels, plus two analog output channels. The DVME-691D accommodates up to eight analog output channels.

As supplied by the factory, signals pass from the screw terminals to specific flat ribbon connectors via etched circuitry. The user's sensor, transducer, and actuator cabling connects to screw terminals on the top portion of the DVME-691's. Prior to passing the signals on to the VMEbus cards, the user may introduce signal conditioning circuitry using the provided etch layout. The user solders in discrete components per the application requirements, cutting the etch (where necessary) which normally connects the input to the output connectors.

The DVME-691A and DVME-691D include five-foot-long flat cables used to pass the signals directly to DATEL's DVME-600 Series of high-performance VME A/D and D/A boards.

The mounting bracket, included in both versions, also has a Plexiglas safety shield which accommodates labeling requirements.

Two Versions for A/D or D/A

The DVME-691A and DVME-691D differ only in the placement and pinout of mating flat cable connectors. For analog inputs, model DVME-691A accepts up to 32 single-ended or 16 differential inputs, as supplied by DATEL's 32S/16D-channel DVME-611 or DVME-601 A/D board. The DVME-691A has two additional channels designated as analog output channels when using DATEL's DVME-612 combination A/D-D/A board.

For analog input channel expansion (up to 256 channels), the DVME-691A also works with DATEL's DVME-641 and DVME-645 slave analog input multiplexer channel expander boards. These expanders share the same A/D converter on the A/D master board, offering low channel costs and a simple means of adding more channels.

For analog outputs, Model DVME-691D distributes up to 8 D/A channels. The DVME-691D is directly compatible with DATEL's DVME-624, -626, -628 and -620 Series D/A boards.

Ordering Information
See Last Page

FUNCTIONAL SPECIFICATIONS

(Apply to the DVME-691A and DVME-691D unless otherwise noted.)

DVME-691A

Number of Analog Input Channels . . . . 32 single-ended or 16 differential plus 2 DVME-612 D/A channels.

Connections per Channel . . . . . Hi, Lo, Ground (Differential) and G,H,H,G,H,H, ... (Single-ended). Single-ended inputs share one ground for every two channels. There are 48 A/D terminals, total.

There are 4 screw terminals for the DVME-612 D/A outputs.

DVME-691D

Number of Analog Output Channels . . . 8 voltage outputs or current loops.

Connections per Channel . . . . . Voltage output, voltage return, current loop voltage, current loop output, current loop return. There are 5 terminals per D/A channel.

DVME-691A and DVME-691D

Screw Terminal Type . . . . . Barrier terminals using 6-32 screws on 0.325″ centers, suitable for lugs or bare wire, 16 gauge or smaller.

Mating Cables . . . . . Two 25-conductor flat cables are included to mate with DATEL's DVME-600 Series boards. The board end includes a DB-25P connector. The DVME-691 end includes a 26-pin self-keying flat cable header connector. Cable length is five feet.

The 691A also includes a five foot, 10-pin flat cable and DB-9P connector for the 2 DVME-612 D/A channels.

Front Safety Shield . . . . . 0.125″ thick Plexiglas shield accepts user terminal labelling. Remove shield for signal conditioning component installation.

Signal Conditioning . . . . . Component Pads accept user-supplied passive components for voltage attenuation, current shunt, RC filters, protective clamps, loop excitation, etc.

DC Power Rails . . . . . Bipolar DC power from a user-supplied power supply is distributed to all channels for loop excitation, clamps, etc. The rails are brought out to screw terminals for power supply connection.

Outline Dimensions . . . . . 19″ W x 3.5″ H x 4.62″ D with mounting slots on 3″ vertical centers and 18.5″ horizontal centers. (Suitable for 19″ RETMA rack mounting).

Operating Temperature . . . . . 0 to +70 degrees Celsius

COMPATIBILITY TABLE

TERMINATOR	USED WITH	TOTAL NUMBER OF CHANNELS
	Analog Inputs	
DVME-691A	DVME-601	16S or 8D A/D
DVME-691A	DVME-611/612	32S or 16D A/D plus 2 D/A
DVME-691A	DVME-641	32S or 16D Slave multiplexing A/D*
DVME-691A	(2) DVME-645	16S or 8D Simultaneous sample/hold*
	Analog Outputs	
DVME-691D	(2) DVME-624	8 Isolated D/A or 4-20 mA loop outputs
DVME-691D	DVME-626	6 High-resolution D/A
DVME-691D	DVME-628	8 D/A or 4-20 mA loop outputs

* (The slave MUX boards require a host DVME-611 or 612 A/D board).

DATEL's DVME-602 and DVME-643 boards include their own screw terminal interfaces and do not connect to the DVME-691.

Signal Conditioning Component Pads

DATEL ships the DVME-691 with straight-through connections between external devices and analog channels. However, the DVME-691 easily adapts to an extensive variety of signal conditioning circuits. Circuits consisting of passive components (resistors, capacitors, diodes, etc.) install directly on the 691's printed circuit board using etch provided.

The plated-through PC board pads are pre-drilled and clearly identified by screening labels. As configured, the pads support circuits for input attenuation, current shunt input (including 4-to-20 mA applications), noise filtering, and overvoltage protection clamps.

OUTLINE DIMENSIONS IN (mm)
(TOP VIEW)

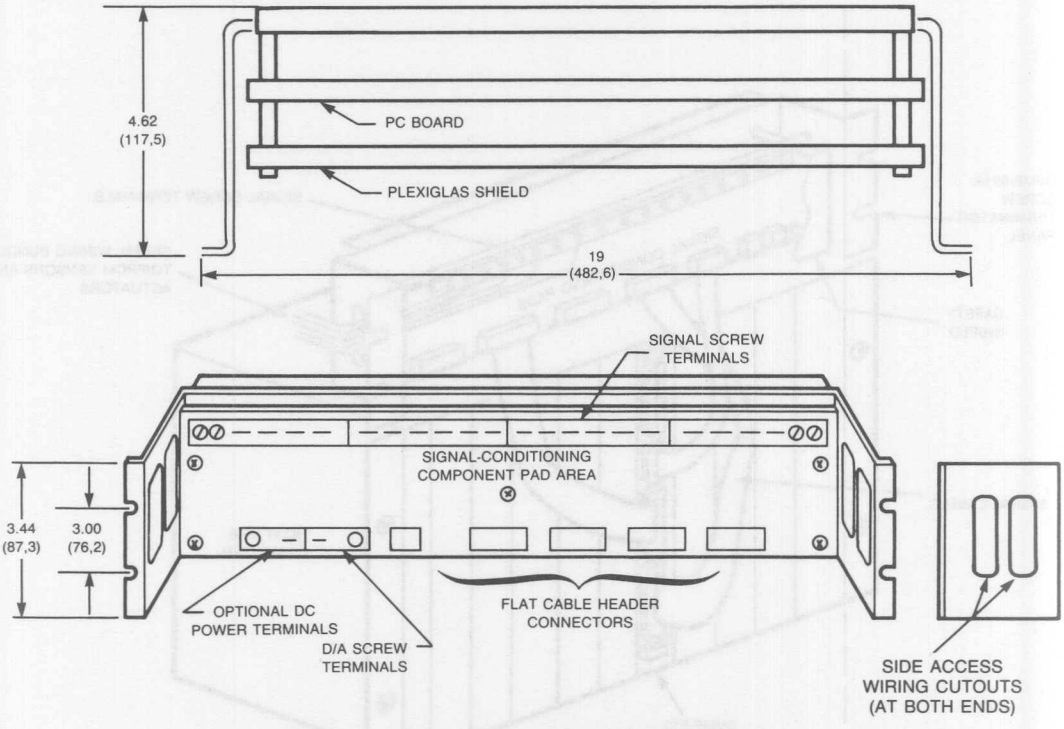


Figure 1. Connector Locations/Dimensions

DC Power Rails

Adjacent to each channel are bipolar dc power supply rails. These may be used for clamp circuits, for sensor excitation, or open-circuit detection. The dc rails are brought out to screw terminals suitable for connection to an adjacent dc power supply. There is ample room to mount a supply on standoffs on the rear of the DVME-691. Voltages up to ±15V dc may be distributed to each channel.

For D/A outputs, the signal conditioning pads could be used for excitation of 4-to-20 mA current loops. Such excitation circuits would use the dc power supply, the distributed dc rails, and current-excitation resistors on a per-channel basis.

Signal Conditioning Circuitry

Signal-conditioning circuitry can be of the user's design or DATEL can provide the design, testing, and installation of such circuitry under special quantity order.

Sensor Families

As configured, the DVME-691A is ideal for voltage and millivolt-input sources. These include bridges, strain gages, load cells, and RTD's. The DVME-691 adapts to 4-to-20 mA loop inputs by adding current loop shunts. The DVME-691A accepts thermocouple inputs if the user supplies external cold junction compensation (CJC).

Alternatively, electronic CJC may be provided on the A/D board by using DATEL's Model DVME-602T or DVME-643T slave thermocouple channel expander boards. These two products include their own front panel screw terminals.

OTHER FEATURES

The DVME-691 is intended for factory-floor, industrial, and laboratory applications. As shown in Figure 1, the screw terminals accept field signal wiring either as bare wire or terminated with strain-relieved lugs. Access holes in the sides of the DVME-691 permit routing the wiring through the rear of the DVME-691. Because of this access, several DVME-691's can mount above each other in the same rack or directly adjacent to the host A/D-D/A computer.

The DVME-691 also includes a transparent safety shield which prevents accidental contacts while providing a means of labelling each connection. The DVME-691 does not protrude from the rack.

TYPICAL RACK-MOUNT APPLICATION

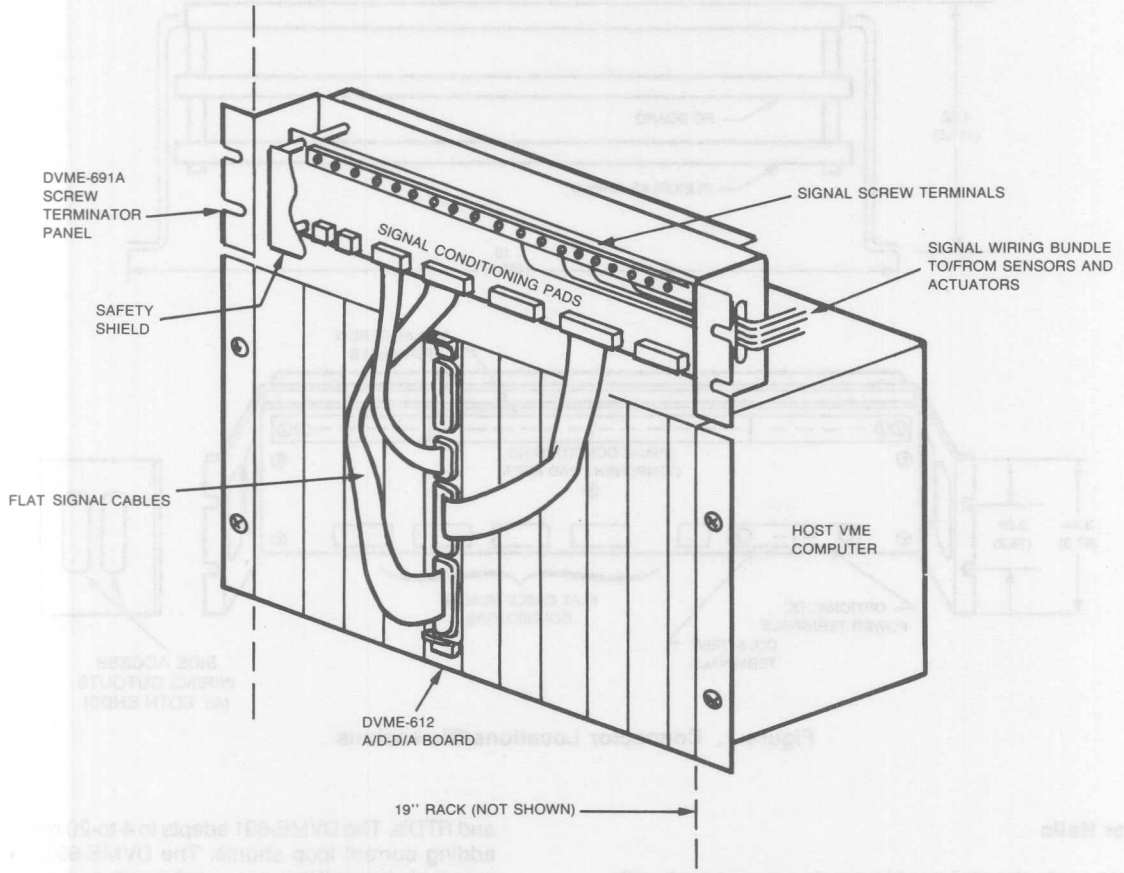


Figure 2. Typical Rack-Mount Configuration

Typical Rack Mount Application
(Figure 2)

This diagram shows the DVME-691 mounted in a 19″ rack adjacent to its host computer. Three supplied flat cables connect the DVME-691 to a Model DVME-612 combination A/D-D/A board. The DVME-691 may be positioned either above or below the computer. The cables are each one meter long so that, if required, the 691 may be located in an adjacent rack.

Before connecting the field wiring, the 691's PC board is removed for optional signal conditioning component installation by the user. Signal wiring for input sensors and transducers or output devices connects to the screw terminals along the top of the DVME-691. This wiring may be collected in bundles and routed either through the slots at the ends of the DVME-691 or over the top edge. Wire bundle routing through the slots allows adjacent equipment to be rack-mounted immediately above the DVME-691.

This application uses three flat cables — two for A/D signals and the third for the two DVME-612 D/A channels. User-supplied dc power, if required for sensor excitation or protective clamps, would connect to the screw terminals at the lower left corner of the DVME-691. Ample room is available on the rear mounting bracket to attach a small dc power supply.

Signal Conditioning Pads per Channel
(Figure 3)

This drawing shows the arrangement of PC board circuit pads for each analog channel. The user selects and installs suggested components shown in the illustration. (DATEL will review custom applications under special order). The pad area is intended for a wide range of applications and the user does not have to use the components indicated. As supplied, connections are made straight-through from the screw terminals.

DC power rails are bussed to each channel and are brought out to screw terminals.

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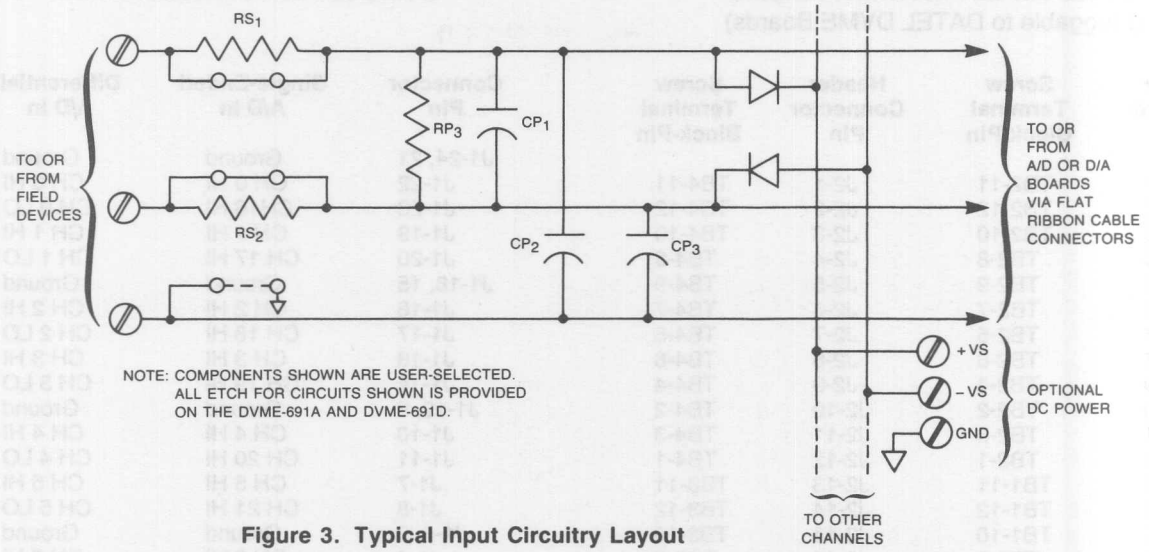


Figure 3. Typical Input Circuitry Layout

Filters and Attenuators

When measuring some signals, it may become necessary to filter out unwanted noise or to attenuate the signals prior to passing them to the analog-to-digital converter board. The DVME-691A provides the user with a convenient area for user-configured passive signal conditioning.

Figures 4, 5, and 6 show typical configurations of simple high-pass, low-pass, and attenuator circuits.

Typical values for a high-pass filter

If the desired cutoff frequency (Fc) is 60 Hz and if Rp is chosen as 10K ohms for differential inputs into the DVME-691,

$$\text{then, } Cs = \frac{1}{2\pi\,(Rp)\,(Fc)} = \frac{1}{2\pi\,(10K)\,(60)} = 0.265\ \mu F$$

Refer to Figure 4, installing a 0.265 μF capacitor in the place of RS1 and a 10K ohm resistor in place of RP3.

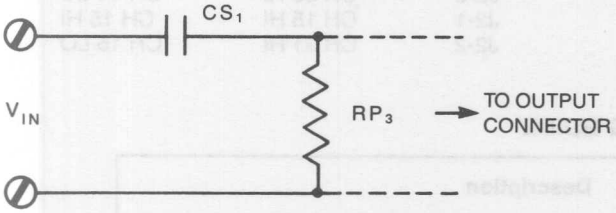


Figure 4. Typical High-Pass Filter

Typical Values For a Low-pass Filter

If the desired cutoff frequency (fc) is 40 Hz, and if Rs is chosen as 20K ohms for single-ended inputs into the DVME-691,

$$\text{then, } Cp = \frac{1}{2\pi\,(Rs)\,(fc)} = \frac{1}{2\pi\,(20K)\,(40)} = 0.2\mu F$$

Refer to Figure 5, installing a 0.2μF capacitor in the place of CP2 and a 20K ohm resistor in place of RS1.

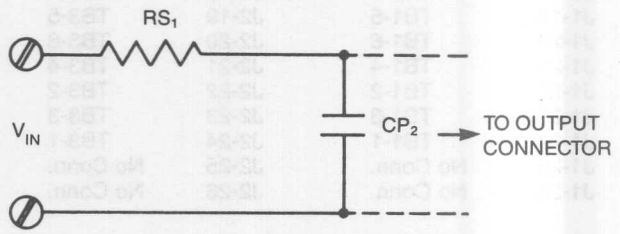


Figure 5. Typical Low-Pass Filter

Typical Attenuator Circuit

If the input signal is 50V dc and the input circuit device can only handle +10V dc maximum, an attenuation circuit can be made up as follows:

If choosing a 100K ohm resistor for Rs,

$$Rp = \frac{Vp\ Rs}{Vin - Vp} = \frac{10(100K)}{50 - 10} = \frac{1\ \text{megohm}}{40} = 25K\ \text{ohms}$$

Refer to Figure 6, installing a 25K ohm resistor in the place of RS3 and a 100K ohm resistor in place of RS1.

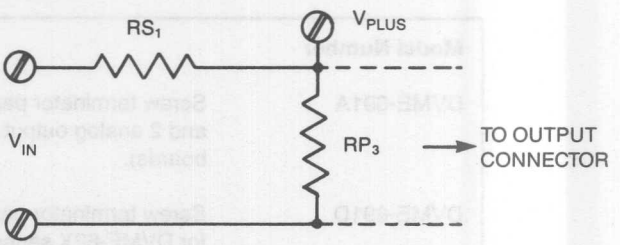


Figure 6. Typical Attenuation Circuitry

DVME-691 26-Pin Header Pinouts
(Pluggable to DATEL DVME Boards)

Header Connector Pin	Screw Terminal Block-Pin	Header Connector Pin	Screw Terminal Block-Pin
J1-1	TB2-11	J2-1	TB4-11
J1-2	TB2-12	J2-2	TB4-12
J1-3	TB2-10	J2-3	TB4-10
J1-4	TB2-8	J2-4	TB4-8
J1-5	TB2-9	J2-5	TB4-9
J1-6	TB2-7	J2-6	TB4-7
J1-7	TB2-5	J2-7	TB4-5
J1-8	TB2-6	J2-8	TB4-6
J1-9	TB2-4	J2-9	TB4-4
J1-10	TB2-2	J2-10	TB4-2
J1-11	TB2-3	J2-11	TB4-3
J1-12	TB2-1	J2-12	TB4-1
J1-13	TB1-11	J2-13	TB3-11
J1-14	TB1-12	J2-14	TB3-12
J1-15	TB1-10	J2-15	TB3-10
J1-16	TB1-8	J2-16	TB3-8
J1-17	TB1-9	J2-17	TB3-9
J1-18	TB1-7	J2-18	TB3-7
J1-19	TB1-5	J2-19	TB3-5
J1-20	TB1-6	J2-20	TB3-6
J1-21	TB1-4	J2-21	TB3-4
J1-22	TB1-2	J2-22	TB3-2
J1-23	TB1-3	J2-23	TB3-3
J1-24	TB1-1	J2-24	TB3-1
J1-25	No Conn.	J2-25	No Conn.
J1-26	No Conn.	J2-26	No Conn.

DVME-691 26-Pin Header Pinout

Connector Pin	Single-Ended A/D In	Differential A/D In
J1-24, 21	Ground	Ground
J1-22	CH 0 HI	CH 0 HI
J1-23	CH16 HI	CH 0 LO
J1-19	CH 1 HI	CH 1 HI
J1-20	CH 17 HI	CH 1 LO
J1-18, 15	Ground	Ground
J1-16	CH 2 HI	CH 2 HI
J1-17	CH 18 HI	CH 2 LO
J1-13	CH 3 HI	CH 3 HI
J1-14	CH 19 HI	CH 3 LO
J1-12, 9	Ground	Ground
J1-10	CH 4 HI	CH 4 HI
J1-11	CH 20 HI	CH 4 LO
J1-7	CH 5 HI	CH 5 HI
J1-8	CH 21 HI	CH 5 LO
J1-6, 3	Ground	Ground
J1-4	CH 6 HI	CH 6 HI
J1-5	CH 22 HI	CH 6 LO
J1-1	CH 7 HI	CH 7 HI
J1-2	CH 23 HI	CH 7 LO
J2-24, 21	Ground	Ground
J2-22	CH 8 HI	CH 8 HI
J2-23	CH 24 HI	CH 8 LO
J2-19	CH 9 HI	CH 9 HI
J2-20	CH 25 HI	CH 9 LO
J2-18, 15	Ground	Ground
J2-16	CH 10 HI	CH 10 HI
J2-17	CH 26 HI	CH 10 LO
J2-13	CH 11 HI	CH 11 HI
J2-14	CH 27 HI	CH 11 LO
J2-12, 9	Ground	Ground
J2-10	CH 12 HI	CH 12 HI
J2-11	CH 28 HI	CH 12 LO
J2-7	CH 13 HI	CH 13 HI
J2-8	CH 29 HI	CH 13 LO
J2-6, 3	Ground	Ground
J2-4	CH 14 HI	CH 14 HI
J2-5	CH 30 HI	CH 14 LO
J2-1	CH 15 HI	CH 15 HI
J2-2	CH 31 HI	CH 15 LO

ORDERING GUIDE

Model Number	Description
DVME-691A	Screw terminator panel for 32 single-ended or 16 differential analog input and 2 analog output channels (includes 3 cables for DVME-611/612 boards).
DVME-691D	Screw terminator panel for 8 analog output channels (includes 2 cables for DVME-62X series boards).

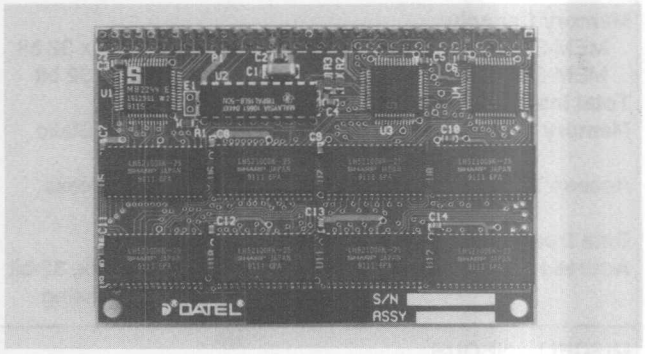
Contact DATEL for custom component configurations

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INNOVATION and EXCELLENCE

MEM-30
Very High-Speed A/D Memory Expansion Module

FEATURES

- **Memory expansion for DATEL's PC-430 or DVME-630 A/D-DSP boards**
- **High-density, 1M x 32 bit, static RAM capacity**
- **Very high-speed memory - 25ns access time**
- **Full 32-bit data bus**
- **Low power from carrier motherboard**
- **TTL-compatible inputs and outputs**
- **Low-profile surface mount technology**



GENERAL DESCRIPTION

MEM-30 is a high-speed static RAM daughter board that offers up to 4 additional megabytes of local Digital Signal Processor (DSP) memory to DATEL's intelligent analog input boards. Total installed capacity is 4.5 megabytes. MEM-30 is constructed using eight 128k x 8 bit or 512k x 8 bit high-density SRAM's mounted on a compact, low-profile pluggable module. The module is pin-compatible with the DSP primary memory bus connector on the PC-430 (for PC/AT bus) and DVME-630 (for VME bus) A/D-DSP coprocessor boards.

MEM-30 is read/write accessible to the local TMS320C30 DSP over a full 32-bit data path. Fast, efficient design and full static operation using 25 nanosecond SRAM's ensure DSP access at full speed with no wait states. This allows optimum A/D data storage and processing rates for high-speed, real time data acquisition applications. All power and control is taken from the carrier motherboard, and the expansion card is placed in a low-power standby mode when deselected.

The memory on the expansion board is local DSP memory and is not hardwired to the host computer's address and data busses. The board appears as a block of memory locations in the DSP address range 20000 hex to 11FFFF hex. Programmable array logic (PAL) address decoders interpret the higher order addresses and steer the data to/from the correct memory locations.

The host computer system may access MEM-30 data through the Dual Port RAM (DPR) on the carrier motherboard. A high-speed, command list form of DSP control called Application Function Block (AFB) programming is available for both the PC-430 and DVME-630 boards. These AFB's use a library of TMS320C30 software routines which are downloaded to the DPR where they run at full DSP speed. AFB routines are available that allow the host bus access to the expansion memory data via the DPR.

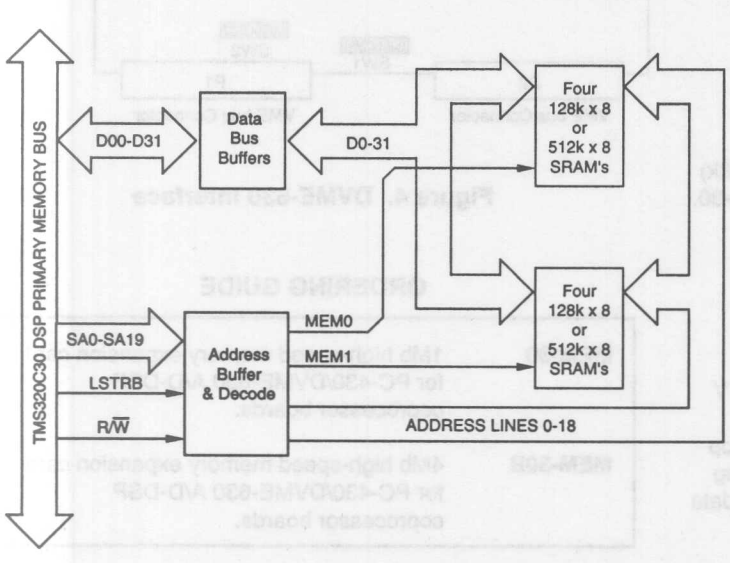


Figure 1. MEM-30 Functional Block Diagram

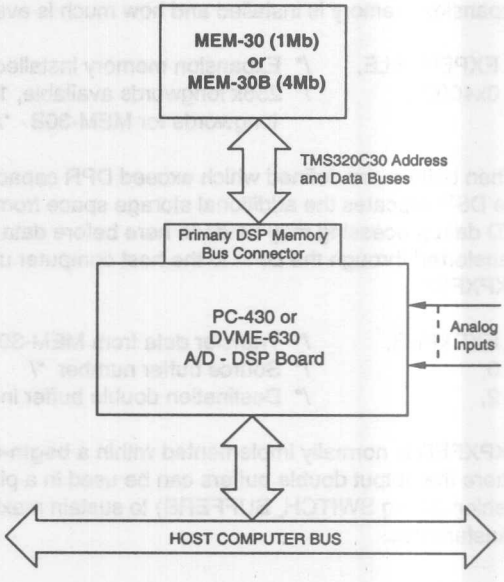


Figure 2. A/D-DSP Board Interface

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C unless otherwise noted)

MEMORY SPECIFICATIONS	
Memory Capacity:	
MEM-30	1Mb, organized as 256k x 32 bit
MEM-30B	4Mb, organized as 1M x 32 bit
Total Installed Memory	Up to 4.5Mb
Memory Type	Very high-speed CMOS Static RAM
Access Time	25ns, 32/40MHz DSP access with no wait states
Data Bus Width	32 bits
Address Range	20000 hex to 11FFFF hex, 32-bit TMS320C30 DSP addressing
MISCELLANEOUS	
Motherboard Connector	72-pin, dual row header connector, TTL levels. Compatible with DSP primary memory connector on DATEL's PC-430 and DVME-630 A/D-DSP coprocessor boards.
Power Required	+5V dc at 0.5 Amps maximum. All power supplied by host carrier motherboard.
Operating Temp. Range	0 to +60°C
Storage Temp. Range	-25 to +85°C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet
Outline Dimensions	3.625 x 2.5 x 0.1875 in. (9.208 x 6.35 x 0.476 cm)
Weight	1.3 ounces (37 grams)

AFB Programming for MEM-30

Two AFB functions are available for use with the MEM-30's, EXPENABLE and EXPXFER. The former tells the DSP that expansion memory is installed and how much is available:

```
EXPENABLE,      /* Expansion memory installed */
0x40000,        /* 256k longwords available, 1M
                   longwords for MEM-30B */
```

When buffers are defined which exceed DPR capacity (128k) the DSP allocates the additional storage space from MEM-30. A/D data processing may be done here before data is transferred through the DPR to the host computer using EXPXFER.

```
EXPXFER,        /* Transfer data from MEM-30 */
0,              /* Source buffer number */
2,              /* Destination double buffer in DPR */
```

EXPXFER is normally implemented within a **begin-end** loop where the output double buffers can be used in a ping-pong fashion (using SWITCH_BUFFERS) to sustain maximum data transfer rates.

MEM-30 INSTALLATION

Expansion memory SRAM's and control logic are surface mounted on a pluggable daughter module which interfaces to the motherboard through a 72-pin, dual-row, female header connector. This mates with the corresponding primary memory bus connector on the PC-430 and DVME-630 as illustrated. Orient the module correctly and carefully press into place. Incorrect alignment will bend or damage connector pins.

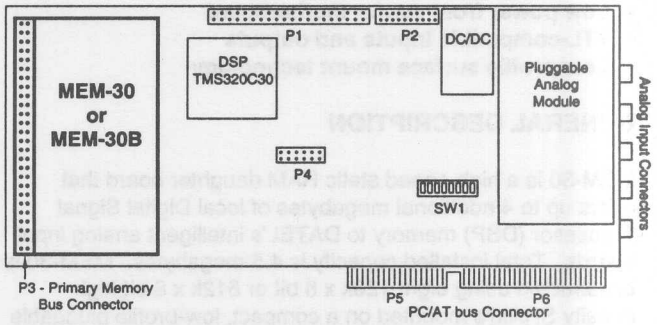


Figure 3. PC-430 Interface

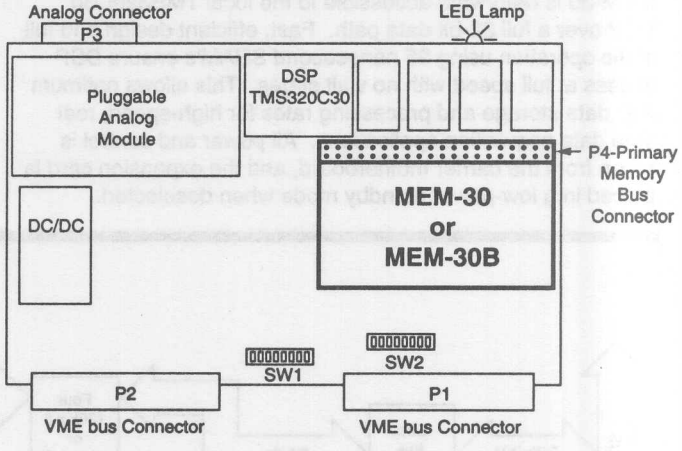


Figure 4. DVME-630 Interface

ORDERING GUIDE

MEM-30	1Mb high-speed memory expansion card for PC-430/DVME-630 A/D-DSP coprocessor boards.
MEM-30B	4Mb high-speed memory expansion card for PC-430/DVME-630 A/D-DSP coprocessor boards.

INNOVATION and EXCELLENCE

High Quality Boards for Multibus I

Easily the grandfather of all microcomputer buses, Multibus I continues its widespread usage around the globe. Begun in the 1970's as part of Intel's MDS-800 Development System (using an 8080 CPU and never intended as a board family!), Multibus eventually exceeded everyone's expectations for industry-wide acceptance. Its clearly written IEEE standard, ease of use, and effective low-cost software were the major factors in transforming the minicomputer market into the microprocessor revolution. By the time the IBM-PC appeared in the early 1980's, Multibus was at the heart of everything from engine test diagnostic systems to NASA photoimaging equipment.

In many emerging countries, Multibus boards are still being designed in because they are an exceptionally well-proven, very reliable system for industrial automation and process control. It's the bus that won't die! Multibus is simple to use, easy to understand, and troubleshooting does not require exotic equipment. In major markets around the world, cost-effective, proven Multibus systems continue to be maintained and duplicated with no overriding reason to design in newer buses.

DATEL continues to offer high-quality, thoroughly tested Multibus boards with full product support. While Multibus is not generally recommended for new high-performance applications, several CPU manufacturers continue to install new CPU's on Multibus and upgrade to the most current software. The latest technology retains full downward compatibility to all levels of earlier Multibus products.

Multibus Selection Table 3-2
ST-519 3-3
ST-703 3-9
ST-711/732 3-13
ST-716 3-19
ST-728 3-25

Multibus I Selection Tables

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INNOVATION and EXCELLENCE

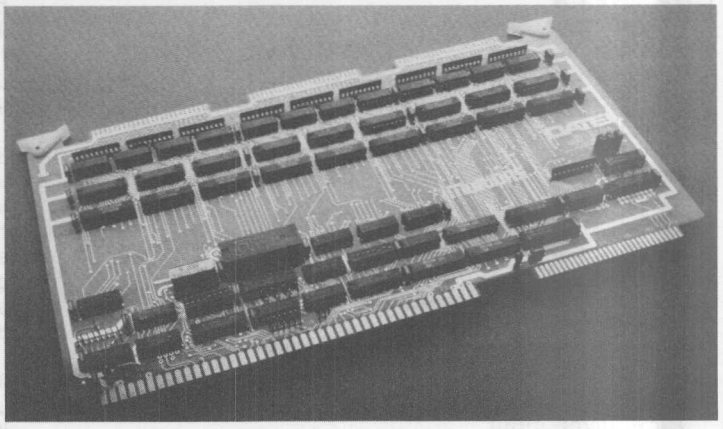
Multibus I Analog Boards

Model	I/O Channels	I/O Ranges	A/D or D/A Resolution	Conversion Rate	Notes
ST-711	32SE/16D A/D	50mV to 10V	12 bits	23kHz	16/20/24-bit Multibus host, programmable pacer clock
ST-732	32SE/16D A/D, 2 D/A	50mV to 10V	12 bits	23kHz	16/20/24-bit Multibus host, programmable pacer clock
ST-703	4 D/A isolated	0 to +5V, +10V	12 bits	167kHz	Channel-to-channel isolated 300V, 8/16-bit transfer
ST-716	4 or 8 D/A	0 to +10V, ±5V, ±10V	16 bits	38kHz	16/20/24-bit Multibus host, ±0.005% linearity
ST-728	4 or 8 D/A	0 to +10V, ±5V, ±10V, 4-20mA	12 bits	200kHz	16/20/24-bit Multibus host, passive current loops, 15-36V external excitation
ST-519	72-line digital I/O	TTL logic	—	To 4Mb/sec	16/20/24-bit addressing, programmable direction by byte, interrupt control

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ST-519
MULTIBUS, 72-Line Digital I/O Board with Interrupt



FEATURES

- **72 Individually-programmable input/output lines**
- **IEEE 796 MULTIBUS Compatible**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Memory mapped, optional I/O map**
- **16-, 20- or 24- bit user-selectable base address**
- **Eight maskable interrupt lines**
- **Interfaces to pluggable modules for 2.5KV isolation**

DATEL expands its line of MULTIBUS compatible system boards with the ST-519. The ST-519 provides 72 individually-programmable lines for input or output (I/O). Also, an interrupt controller is provided to allow up to eight user-programmable interrupt lines. Like other DATEL MULTIBUS products, the ST-519 is fully hardware- and software-compatible with all MULTIBUS microcomputers. All necessary address decoders, logic controls, and data transceivers are incorporated on board.

DESCRIPTION

The DATEL ST-519 is a MULTIBUS-compatible system board providing 72 software programmable input/output (I/O) lines. These I/O lines are fully TTL compatible and each line can be individually programmed as either an input or an output.

The ST-519 may be used with both 8- and 16-bit microprocessors. The BHEN/line on the MULTIBUS sets the ST-519's address decoders and data latches for compatibility with 8- or 16-bit computers. The ST-519 also supports 24-bit MULTIBUS addressing capability, and is downward compatible with 16- or 20-bit address systems.

The ST-519 has an 8259A Programmable Interrupt Controller which provides vectoring information for eight user-definable interrupt levels. In normal slave operation, the Interrupt Request (IR) lines of the 8259A are hard-wired to an I/O line. When the I/O event occurs the 8259A generates an Interrupt (INT) which would go to one of the MULTIBUS vector interrupt lines INTØ thru INT7.

The 72 I/O lines are brought out on three 50-pin edge-card connectors: J1, J2, and J3. These edge-card connectors are fully compatible to the Gordos and OPTO 22 type pluggable modules systems that offer an input to output isolation of 2.5K VAC. A flat ribbon cable interconnects the DATEL ST-519 to other electronic module systems.

The ST-519 is a memory-mapped peripheral occupying 16 consecutive locations in the computer's address space. The board's base address is preset at ØØFFAØ hex. However, a user may relocate the board address anywhere up to FFFFFØ on 16-byte boundaries using DIP switches on the board.

In order to make the ST-519 compatible with different speed CPU and memory systems, a transfer acknowledge delay (XACK/DELAY) is provided. This permits 8 selectable delays from 100 to 800 nanoseconds.

The ST-519 is fully bus- and card-cage compatible with the MULTIBUS and IEEE 796. The board is 12.0"W x 6.75"D x 0.47"H (305 x 172 x 12 mm). When used with the standard MULTIBUS card cage, the ST-519 board may be installed adjacent to other boards.

The ST-519 draws all power from the MULTIBUS +5V dc power line. The ST-519 weighs approximately 12 ounces (0,341 kg). It can operate over a temperature range of 0 to +55 degrees Celcius with relative humidity from 10 to 90% (noncondensing), and from 0 to 15,000 feet (0 to 4,600 m) in altitude.

Compatible to Opto-22, PB-16, or PB-24 I/O panels or equivalent.

ORDERING GUIDE

MODEL	DESCRIPTION
ST-519	72 line digital I/O board with interrupt

FUNCTIONAL SPECIFICATIONS

CHANNELS

I/O number of channels..... 72 I/O Channels
Channel expansion.... Indefinite channel expansion using separate ST-519 boards at different base addresses; limited by available card slots and supply current

OUTPUT DRIVER

Output current sink (Vout = 0.6V)..... 24 mA (max.)
Output current source (Open collector 4.7KΩ from +5V)..... 1 mA (max.)

INPUT RECEIVER

High level input current (Vin = 2.7V).....100 µA (max.)
Low level input current (Vin = 0.4V).....-1.2 mA (max.)

ADDRESSING

Occupies a block of 16 consecutive memory (I/O) locations. Base address may be located on any 16 byte boundary in the 16-, 20- or 24-bit address space by two DIP switches.

PHYSICAL

Outline Dimensions... 12.00"W x 6.75"D x 0.50"H (max.)
304,8W x 171,5D x 12,7H mm
Weight..... 12 ounces (0.34 kg)
Operating Temperature Range..... 0 to +55°C
Storage Temperature Range..... -25 to +85°C
Relative Humidity..... 10% to 90% non-condensing
Altitude..... 0 to 15,000 feet (4,600 m)

POWER CONSUMPTION +5V dc ±5%

ST-519 (stand alone)..... 1.7 A typical
ST-519 + 72 I/O modules.....3.3 A typical

GENERAL

Bus Compatibility..... Pin-for-pin, card guide, and program compatible with MULTIBUS (IEEE 796) and SBC series microcomputers
CPU Compatibility.....8 or 16 bit compatible

DATA FORMAT

The ST-519 is a memory-mapped peripheral that appears to the system CPU as 16 bytes of consecutive memory. These registers can be accessed as 16 single bytes (8-bit CPU) or as 8 double bytes (16-bit CPU).

The ST-519 board automatically changes to a 16-bit format when the BHEN/line on the MULTIBUS pin 27 of connector P1 goes to zero volts. A high input on BHEN/, consequently, sets the board for an 8-bit format.

INTERRUPT

An 8259A Programmable Interrupt Controller provides onboard interrupt generation to the host's interrupt controller. This device generates interrupts on low-to-high transitions from user-selected digital inputs coming into the ST-519. Jumpers (pins 64 through 71) tie the selected digital input lines directly to the selected IR interrupt.

Jumper pins 64 through 71 have two different uses based upon the mode of operation. In one mode, the MULTIBUS interrupt priority level (INT 0-7) is jumper-selectable between pin 111 (INT) and the jumper pins for the priority levels as outlined below (pins 103, 104, 105 . . .). For this single-interrupt scheme, the user wires the interrupt source to an interrupt input pin (pins 64 through 71). Jumper pins 97 through 101, 109 and 110 are not used in this mode.

In the other mode, up to eight interrupt levels are defined using eight digital input bits to the ST-519. Each input has a jumper, pins 97 through 113 (excluding 111). Pins 64 through 71 are user-prioritized and connected (through buffers and jumpers) to the MULTIBUS INT 0-7 lines. This mode bypasses the 8259A and its interrupt vector address function. Use this mode when the host provides the necessary vectoring information for servicing the interrupt caused by the digital input.

8259A		MULTIBUS	
Line Name	ST-519 Jumper Pin#	Line Name	ST-519 Jumper Pin#
INT	111	INT0	112
IR0	67	INT1	113
IR1	68	INT2	107
IR2	66	INT3	108
IR3	71	INT4	105
IR4	65	INT5	106
IR5	70	INT6	103
IR6	64	INT7	104
IR7	69		

CONNECTORS

The ST-519 board contains five connectors: P1 and P2 are the MULTIBUS connectors, and J1, J2, and J3 are the digital I/O connectors.

The P2 MULTIBUS connector is used only when a system controller's address capability is 24 bits. The pin assignment for the four extended address lines on P2 are shown in Table 1.

The digital I/O lines use connectors J1, J2, and J3; Table 2 describes these connections.

Table 1. MULTIBUS Connector P2

PIN	SIGNAL	Functional Description
55	ADR 16	
56	ADR 17	4 address line inputs for 24
57	ADR 14	bit address controllers
58	ADR 15	

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Table 2. I/O Connector

Connector Pin Number	J1 Register Addr	J1 Bit	J2 Register Addr	J2 Bit	J3 Register Addr	J3 Bit	I/O Module	Connector Pin Number	J1 Register Addr	J1 Bit	J2 Register Addr	J2 Bit	J3 Register Addr	J3 Bit	I/O Module
2	2	7	5	7	8	7	23	26	1	3	4	3	7	3	11
4	2	6	5	6	8	6	22	28	1	2	4	2	7	2	10
6	2	5	5	5	8	5	21	30	1	1	4	1	7	1	9
8	2	4	5	4	8	4	20	32	1	0	4	0	7	0	8
10	2	3	5	3	8	3	19	34	0	7	3	7	6	7	7
12	2	2	5	2	8	2	18	36	0	6	3	6	6	6	6
14	2	1	5	1	8	1	17	38	0	5	3	5	6	5	5
16	2	0	5	0	8	0	16	40	0	4	3	4	6	4	4
18	1	7	4	7	7	7	15	42	0	3	3	3	6	3	3
20	1	6	4	6	7	6	14	44	0	2	3	2	6	2	2
22	1	5	4	5	7	5	13	46	0	1	3	1	6	1	1
24	1	4	4	4	7	4	12	48	0	0	3	0	6	0	0

1–49: All odd number pins are tied to ground.

REGISTER

The following chart details the memory address assignments of the 16 memory locations the ST-519 occupies. Please note that when the ST-519 is used with 16-bit CPU's, every other (even-numbered) address location is used.

ST-519 Register Assignments

8 BIT CPU ADDRESS	FUNCTION	REGISTER	COMMENTS	ADDRESS (16 BIT CPU)
BASE + 0	WRITE	WRITE OUTPUT 0–7	REG 0 J1	
BASE + 0	READ	READ INPUT 0–7		BASE + 0
BASE + 1	WRITE	WRITE OUTPUT 8–15	REG 1 J1	
BASE + 1	READ	READ INPUT 8–15		
BASE + 2	WRITE	WRITE OUTPUT 16–23	REG 2 J1	
BASE + 2	READ	READ INPUT 16–23		BASE + 2
BASE + 3	WRITE	WRITE OUTPUT 24–31	REG 3 J2	
BASE + 3	READ	READ INPUT 24–31		
BASE + 4	WRITE	WRITE OUTPUT 32–39	REG 4 J2	
BASE + 4	READ	READ INPUT 32–39		BASE + 4
BASE + 5	WRITE	WRITE OUTPUT 40–47	REG 5 J2	
BASE + 5	READ	READ INPUT 40–47		
BASE + 6	WRITE	WRITE OUTPUT 48–55	REG 6 J3	
BASE + 6	READ	READ INPUT 48–55		BASE + 6
BASE + 7	WRITE	WRITE OUTPUT 56–63	REG 7 J3	
BASE + 7	READ	READ INPUT 56–63		
BASE + 8	WRITE	WRITE OUTPUT 64–71	REG 8 J3	
BASE + 8	READ	READ INPUT 64–71		BASE + 8
BASE + 9	—	NOT USED		
BASE + A	WRITE	CLEAR OUTPUT REG 0–7	CLR REG 0	
BASE + A	READ	READ CLEAR REG		BASE + A
BASE + B	WRITE	CLEAR OUTPUT REG 8	CLR REG 1	
BASE + B	READ	READ CLEAR REG		
BASE + C	WRITE	CONTROL REG 1, 8259A	8259A	
BASE + C	READ	STATUS REG 1, 8259A	INTERRUPT	BASE + C
BASE + D	—	—	CONTROLLER	
BASE + D	—	—	Refer to INTEL data sheet	
BASE + E	WRITE	CONTROL REG 2, 8259A		
BASE + E	READ	STATUS REG 2, 8259A		BASE + E
BASE + F	—	—		
BASE + F	—	—		

CLEAR REGISTERS

The clear registers are used to clear (reset) the output registers to all 0's. On power-up or system reset, the clear register bits reset all output registers which disables all output lines. Only after the clear register bits have been set to 1's will the output (write) function be enabled.

The clear registers format is shown. Refer to I/O line section for programming of input/output registers.

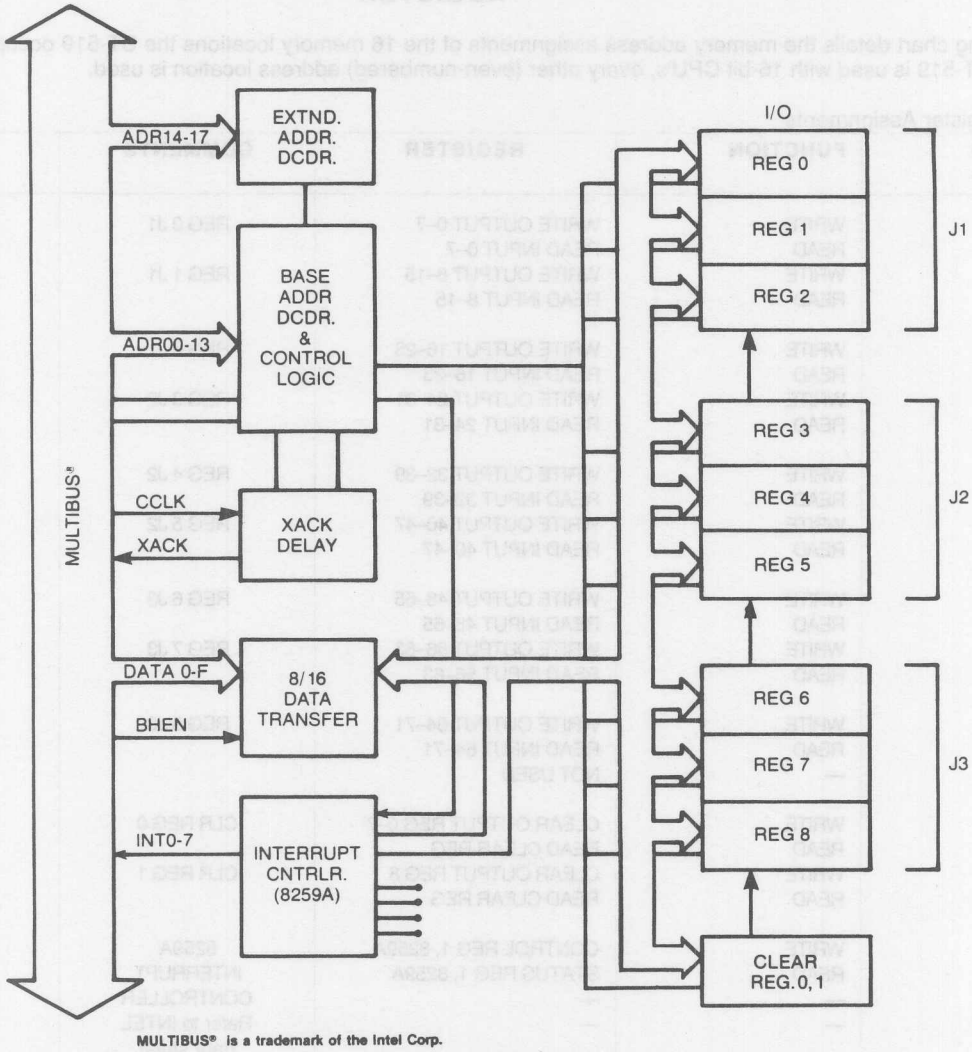
CLEAR REGISTER FORMAT

CLR REG (16 BIT CPU)															
DF															D0
CLR REG 1 (8 BIT CPU)								CLR REG 0 (8 BIT CPU)							
D7							D0	D7							D0
X	X	X	X	X	X	X	X	8	7	6	5	4	3	2	1	0
DON'T CARE								OUTPUT REGISTER CLEARED								

When a clear register bit is 0, the corresponding output register is cleared forcing output lines to logic high (1).

When a clear register bit is 1, the corresponding output register is enabled to be programmed.

ST-519 Block Diagram



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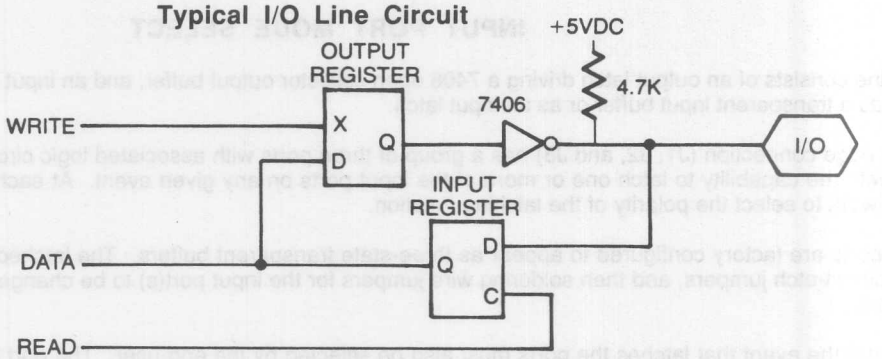
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I/O LINE

All output lines are comprised of an output latch driving an inverting open collector output buffer. During a write cycle to an output register, the data latched will appear inverted at the edge card connector. If the status of an output line is read back thru the ST-519, the previously written data will appear inverted.

An I/O line which is to be used as an input must have its corresponding output line set to a zero. During a read cycle, data from an input line is the true logic level from the edge card connector.

Typical I/O Line Circuit



24 BIT ADDRESS SELECT

The ST-519 is factory configured for 16- or 20-bit addressing. A 24-bit adddress capability is selected by installing programming plugs and soldering a jumper as follows:

1. Cut and remove etch between 46–47.
2. Install wire jumper between 48–47, solder the jumper.
3. Install programming plugs at 75–83, 77–85, 79–87, and 81–89.

BASE ADDRESS SELECTION

The ST-519 is a memory-mapped peripheral that occupies 16 consecutive, byte-wide, memory locations in the computer address space. The base address decoding supports both 16- and 20-bit addressig with 24-bit address capability being optional. Base address selection is accomplished by setting DIP switches on the PC board.

1. Select a base address, in hex, between 000X (00000X) and FFFX (FFFFFX). Write the base address in the Base Address, Hex boxes.
2. Convert the hex code to binary by writing 1's and 0's in the Hex Bit Weighting boxes.
3. Set the desired base address on DIP switch S1 and S2 or the jumper area for extended address. A switch position ON or a wire jumper corresponds to a "1". An OFF switch position or a removed wire jumper corresponds to a "0". If the CPU provides only 16 address lines, the address switches corresponding to ADR10/ through ADR13/ must be left OFF.

BASE ADDRESS HEX	(0 to F)				(0 to F)				(0 to F)				(0 TO F)				(0 TO F)			
HEX BIT WEIGHTING	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
ADDRESS BIT #	17	16	15	14	13	12	11	10	F	E	D	C	B	A	9	8	7	6	5	4
SWITCH/ JUMPER POSITION	84-76	86-78	88-80	90-82	S1 1	S1 2	S1 3	S1 4	S1 5	S1 6	S1 7	S1 8	S2 1	S2 2	S2 3	S2 4	S2 5	S2 6	S2 7	S2 8

I/O SELECT

The ST-519 is factory configured as a memory-mapped peripheral. I/O addressing is an option that may be selected by soldering jumpers by:

1. Cutting and removing etch between 96–93 and 95–91.
2. Installing wire jumpers between 94–93 and 92–91; solder the jumpers.

INPUT PORT MODE SELECT

Each I/O line consists of an output latch driving a 7406 open collector output buffer, and an input device which can be jumper programmed as a transparent input buffer or as an input latch.

Each card edge connection (J1, J2, and J3) has a group of three ports with associated logic circuitry and jumpers to provide the end-user with the capability to latch one or more of the input ports on any given event. At each port group there is an inverter/jumper network to select the polarity of the latching function.

The input ports are factory configured to appear as three-state transparent buffers. The latched input port option is selected by removing circuit-etch jumpers, and then soldering wire jumpers for the input port(s) to be changed. Refer to the Input Port Mode Select chart.

The level and the event that latches the ports must also be selected by the end-user. The port latch event is factory configured to be a positive level (logic level one). A negative level (logic level zero) option is selected by programming plug. The port latch event input must then be hardwired to the event (I/O line, Interrupt Required) that will control the latching of the input port(s).

Refer to the Input Port Mode select chart.

		INPUT PORT		PORT LATCH EVENT		
CONN.	REGISTER	TRANSPARENT (STANDARD)	LATCHED (OPTIONAL*)	POSITIVE (STANDARD)	NEGATIVE (OPTION)	INPUT
J1	REG 0	7-8	8-9	37-43	37-38	49
	REG 1	10-11	11-12			
	REG 2	13-14	14-15			
J2	REG 3	16-17	17-18	39-44	39-40	50
	REG 4	19-20	20-21			
	REG 5	22-23	23-24			
J3	REG 6	25-26	26-27	41-45	41-42	51
	REG 7	28-29	29-30			
	REG 8	31-32	32-33			

*To program to OPTION, first remove etch jumpers under standard and then install and solder option jumpers.

TRANSFER ACKNOWLEDGE (XACK) DELAY SELECTION

The ST-519 generates a transfer acknowledge (XACK/) signal in response to read or write commands from the MULTIBUS. It is sometimes desirable to delay this signal in order to match this signal to the CPU timing. A jumper selectable transfer acknowledge delay ranging from 100 to 800 nanoseconds is available on the ST-519. It should be noted that the XACK/ delay is generated from the MULTIBUS CCLK/ signal which is assumed to have a period of 100 nanoseconds. Also, since this signal is asynchronous, the actual delay can only be set within a tolerance of one clock period or 100 nanoseconds. The accuracy of the XACK/ delay is dependent on the period (T) of the CCLK signal generated by the host computer. The programming of XACK/ delay is in multiple increments of T, ranging from one to a maximum of eight, refer to XACK/ delay selection table below.

DELAY		JUMPERS
100 nsec.		52-53
200 nsec.	(Standard)	52-54
300 nsec.		52-55
400 nsec.		52-56
500 nsec.		52-57
600 nsec.		52-58
700 nsec.		52-59
800 nsec.		52-60

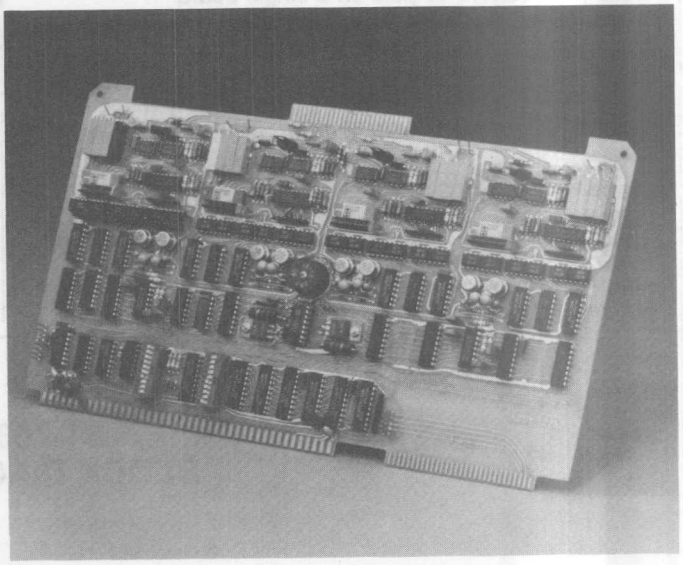
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DATEL®
INNOVATION and EXCELLENCE

ST-703
12-Bit, 4 Channel, Isolated MULTIBUS D/A Board

FEATURES

- **4 D/A Channels using 12-bit monolithic converters**
- **300 VRMS Isolation, channel-to-channel and channel-to-bus**
- **Accurate to .05% of full-scale reading**
- **Uses identical programming and register assignments to SBC-711/732/724 and ST-711/732/724 boards**
- **Includes 4 externally excitation 4-20 mA current loop channels**
- **Memory mapped, with 24-, 20-, or 16-bit user selectable base address**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Complete hardware and software compatibility with MULTIBUS and SBC series microcomputers**



INTRODUCTION

DATEL expands its line of MULTIBUS and SBC compatible analog output boards with the SineTrac ST-703. The ST-703 provides 4 channels of isolated digital-to-analog (D/A) conversion with 12 bits of resolution. Overall voltage output accuracy is within ± .05% of full-scale range. To ensure the board's compatibility with popular process control and test instrumentation, four voltage ranges and a 4-20 mA current loop output are jumper selectable for each D/A channel.

Like other SineTrac products, the ST-703 is fully hardware-and-software-compatible with its host iSBC or MULTIBUS computer. All necessary address decoders, logic controls, and data receivers are built-in. The user installs the ST-703 into an Intel-compatible card cage and wires the analog outputs. The ST-703 is then configured as a memory-mapped peripheral which is addressed by the host computer as eight consecutive memory locations with a user selectable base address. This memory-mapped format allows unlimited D/A channel expansion by using multiple ST-703's, each with a different base address.

The ST-703 is pin compatible with the ST-724, SBC-724, and ST-728 analog output boards. The ST-703 may be used with both 8- and 16-bit microprocessors. The BHEN/line on the MULTIBUS sets the ST-703's address decoders and data latches for compatibility with 8- or 16-bit computers. The ST-703 also supports 24-bit MULTIBUS addressing capability and is downward compatible with 16- or 20-bit systems.

The most unique feature of the ST-703 is its 300 V channel-to-channel and channel-to-bus isolation. Applications include situations where a low-level analog signal must be superimposed on a high voltage, such as testing of power supplies, isolation amplifiers, et cetera. The ST-703 is also useful in applications where actuator failure could cause computer errors or destruction from line voltages being applied to the MULTIBUS. Isolation is accomplished through a combination of optoisolators for digital signals, and transformer isolation for power distribution. An onboard dc-to-dc converter provides four individually isolated supplies for the D/A converters.

The systems manual shipped with each board provides installation instructions, theory of operation, and engineering drawings.

GENERAL DESCRIPTION

Data inputs to the ST-703 are from the host computer's bus. Input coding may be straight binary, offset binary, or 2's complement, and is selectable on the board.

The MULTIBUS BHEN/line is used to set the ST-703's address and data coding for compatibility with 8- or 16-bit CPU's. In the eight-bit mode, the 12 bits of data required for the D/A converters are acquired in two bytes. The lower byte contains the four lower data bits, and is loaded into a storage register for each D/A channel on the ST-703. The next data byte contains the eight higher bits. Upon conversion, the eight MSB's and the four stored LSB's are loaded simultaneously into the DAC. In the 16-bit mode, all 12 data bits are transferred in a single word to the DAC data register. The register outputs are optically isolated and transferred to the D/A converter.

Each channel uses a DATEL model DAC-7541, a 12-bit monolithic device which offers linearity of ± .02% of full-scale range. The converter output is monotonic, having a differential nonlinearity of ± .02% FSR maximum. Offset error on each channel is preadjusted to zero. Trim positions on the board permit recalibration of zero (or offset) and gain settings. Two-speed versions of the board provide settling times of 5 μSec. and 30 μSec. respectively. Zero tempco is ± 2 ppm of FSR/degree Celsius and gain tempco is within ± 10 ppm of FSR/degree Celsius.

The output of each isolated DAC is fed to its own I-to-V conversion amplifier. A total of four voltage output ranges may be jumper selected by the user: 0 to +5V, 0 to +10V, ±5V, and ±10V. In addition, a V-to-I converter circuit is provided for each D/A output channel. A 4 to 20 mA output, usable with an output load from 0 to 500 Ohms, is also jumper selectable.

The ST-703 contains a power-on reset circuit that allows each D/A output to be set to 0.000V at power-on time regardless of the input coding and output range configuration.

The current output requires an external excitation source, a +18V to +30V dc regulated supply capable of 25 mA per D/A channel. Voltage and current ranges on the ST-703 are selected individually for each channel. This allows a mix of voltage or current outputs on a single board.

The ST-703 is a memory-mapped peripheral occupying eight consecutive locations in the computer's address space. The board's base address is factory-set at 00FF10 Hex. However, a user may relocate the board address anywhere up to FFFFF8 on 8-byte boundaries using DIP switches on the board.

To make the ST-703 compatible with different speed CPU's and memory systems, a Transfer Acknowledge Delay (XACK/ Delay) is provided, permitting eight selectable delays from 0 to 700 nSec. in 100 nSec. increments.

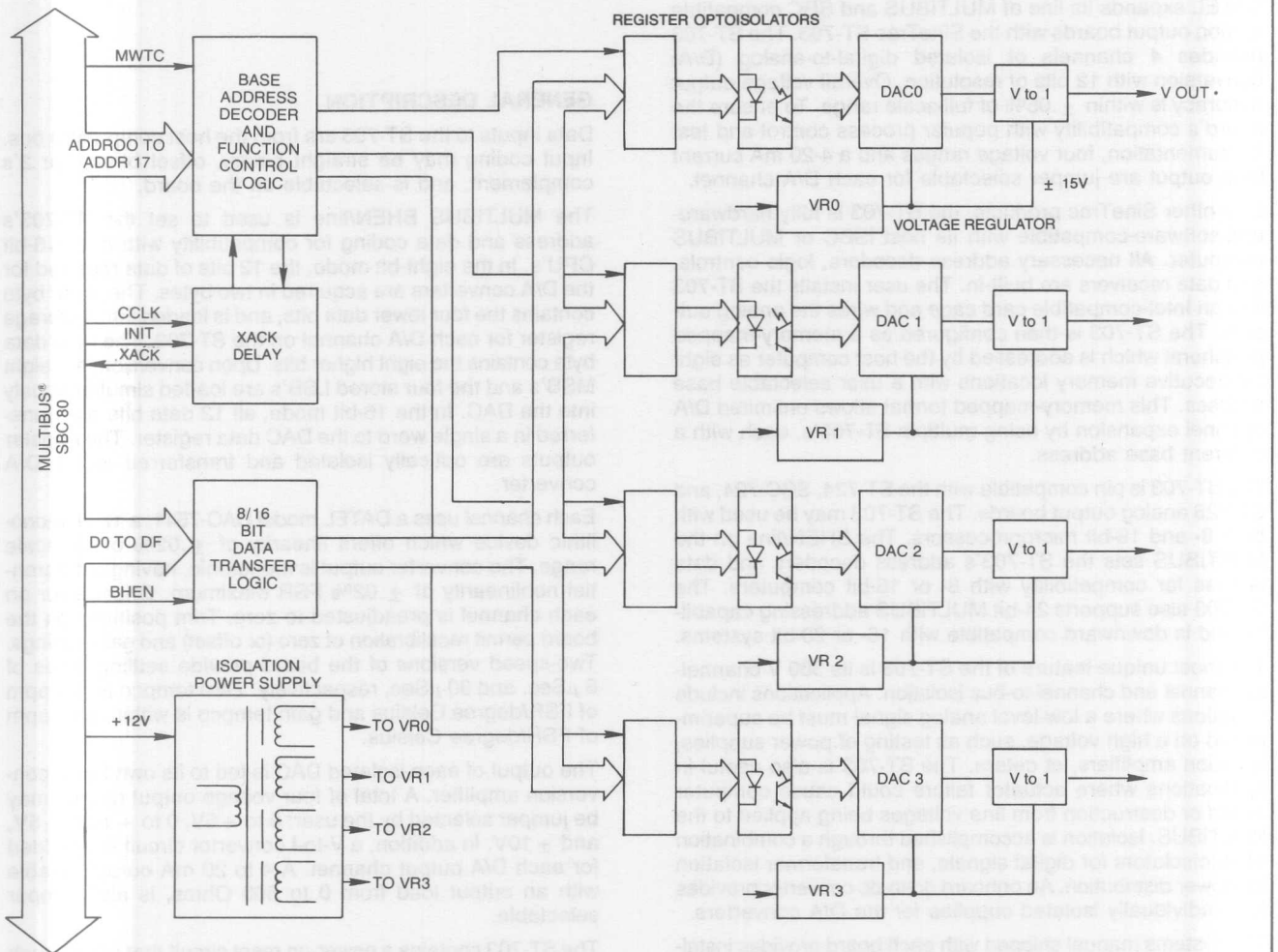
The ST-703 is fully bus-, card cage-, and software-compatible with the MULTIBUS and with Intel RMX software. The board is 12.0 inches wide × 6.75 inches deep × 0.54 inch high (305 × 172 × 14 mm). Multiple ST-703 boards may be mounted in adjacent card slots when used with a standard .60 inch spacing Intel card cage.

The ST-703 draws all its power from the MULTIBUS +5V and +12V lines. An on-board dc-to-dc converter provides four isolated ±15V supplies to drive the analog output circuits.

The ST-703 weighs approximately 12 ounces (0,341 kilograms). It can operate over a temperature range of 0 to +55 degrees Celsius with relative humidity from 10 to 90% (non-condensing), and from 0 to 15,000 feet (0 to 4,600 m) in altitude.

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ST-703
BLOCK DIAGRAM



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FUNCTIONAL SPECIFICATIONS

(typical at 25°C unless otherwise noted) — use generic.

D/A ANALOG OUTPUT

Number of Channels . . 4 D/A channels

Channel Expansion . . . Indefinite channel expansion using separate ST-703 boards at different base addresses; limited by available card slots and supply current

Full-Scale Output Ranges *	±10V (standard) ±5V 0 to +5V 0 to +10V 4 to 20 mA	Individually selectable per channel
Digital Input Coding	Straight Binary Offset Binary (standard) 2's Complement	Selectable per channel
Output Impedance	50 Milliohms	
Output Current (Voltage Output)	Maximum ±5 mA @ ±10V short-circuit-proof to ground.	
Current Loop Excitation Voltage	Maximum +10V to +30V, regulated, user supplied, 25 mA dc maximum channel.	
Isolation Voltage (continuous)	300V RMS channel-to-channel and channel-to-bus	

*NOTE: Outputs are short circuit protected.

ADDRESSING

Reserves a block of eight consecutive memory locations. Base address may be located on an eight byte boundary in the 24-bit CPU address space, provided the least significant byte equals 0 or 8 H.

PERFORMANCE

Accuracy at +25°C	±0.05% of FSR, ±1 LSB (includes noise and nonlinearity).
Differential Nonlinearity	±0.5 LSB, 0 to +55°C
Zero Temperature Drift (Unipolar Output)	Within ±5 ppm of FSR/°C
Offset Temperature Drift (Bipolar Output)	Within ±10 ppm of FSR/°C
Gain Temperature Drift	Within ±20 ppm of FSR/°C
Settling Time	
ST-703B	6 μSec. to 0.5 LSB of final value
ST-703A	30 μSec. to 0.5 LSB of final value
Slew Rate	8 V/μSec.

PHYSICAL

Outline Dimensions	12.00 inches wide x 6.75 inches deep x 0.54 inch high
Weight	304,8 wide x 171,5 deep x 13,7 high mm
Operating Temperature Range	12 ounces (0.34 kilograms)
Storage Temperature Range	−25 to +85°C
Relative Humidity	10% to 90% non-condensing
Altitude	0 to 15,000 feet (4,600 M)

POWER CONSUMPTION +5V @ 1 A
+12V @ 450 mA

GENERAL

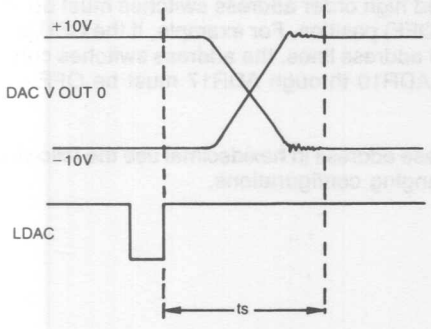
Bus Compatibility	Pin-for-pin, card guide, and program compatible with MULTIBUS (IEEE 796) and SBC series microcomputers.
CPU Compatibility	8- or 16-bit CPU compatible

ORDERING GUIDE

Model ST-703A	Isolated 4 Channel D/A board, 30 μsec. settling time
Model ST-703B*	Isolated 4 Channel board, 5 μsec. settling time

*Note: ST-703B should be selected for applications requiring low transient energy such as amplifier inputs.

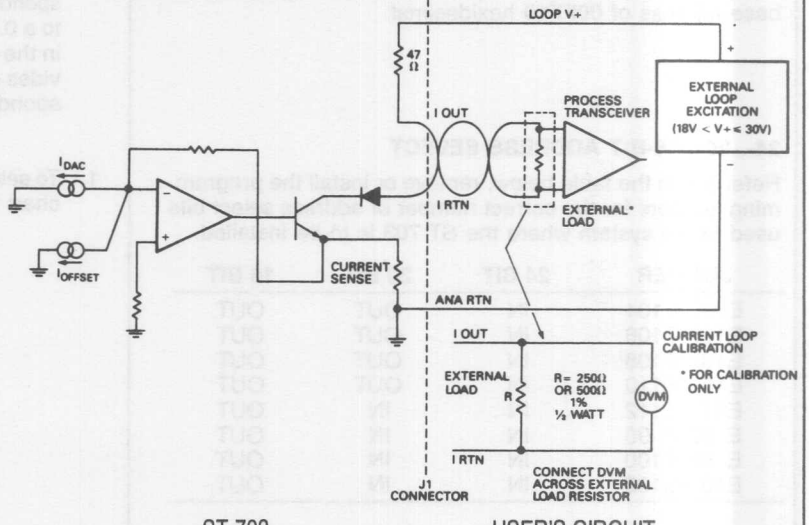
SETTLING TIME



ts: settling time = optoisolator delay + slew time + settling to ±½ LSB final voltage value

Full-scale output ranges*

TYPICAL CURRENT LOOP CIRCUIT



ST-703 USER'S CIRCUIT

DATA FORMAT

The ST-703 is a memory-mapped peripheral and appears to the CPU as a group of eight consecutive memory locations. Two locations are assigned to each D/A channel. The ST-703 requires 12 bits of digital data from the CPU for a single D/A conversion. The following chart shows how 8- and 16-bit CPU's format this data.

The ST-703 board automatically changes to a 16-bit format when the BHEN/line on the MULTIBUS goes to zero volts (pin 27 of the connector P1). Consequently, a high input on BHEN/ sets the ST-703 for the 8-bit format.

D15				SINGLE WORD (16-BIT CPU)			D0								
		HIGH BYTE (8-BIT CPU)								LOW BYTE (8-BIT CPU)					
D7							D0	D7							D0
DAC BIT 1 (MSB)	DAC BIT 2	DAC BIT 3	DAC BIT 4	DAC BIT 5	DAC BIT 6	DAC BIT 7	DAC BIT 8	DAC BIT 9	DAC BIT 10	DAC BIT 11	DAC BIT 12 (LSB)	X	X	X	X

X = Don't care

REGISTERS

Note that 8-bit CPU's must transfer the 12 data bits in two bytes. The low byte contains the four least-significant data bits which are stored in a register on the ST-703. The high byte contains the eight most-significant data bits. When the high byte is transferred, all 12 data bits are loaded into the DAC holding register and the D/A output is updated. Data transfer with a 16-bit CPU is done with a single word transfer; all 12 bits are simultaneously updated. Selection of 8- or 16-bit transfers is accomplished automatically, depending on the state of the MULTIBUS BHEN/line. The following chart details the memory address assignments of the ST-703 board. Note that when the ST-703 is used with a 16-bit CPU, data transfer must be to an even-numbered memory location.

ST-703 REGISTER ASSIGNMENTS

MEMORY ADDRESS (8-BIT CPU)	REGISTER ASSIGNMENT	MEMORY ADDRESS (16-BIT CPU)
BASE + 0	DAC 0 LSB Byte	BASE + 0
BASE + 1	DAC 0 MSB Byte	
BASE + 2	DAC 1 LSB Byte	BASE + 2
BASE + 3	DAC 1 MSB Byte	
BASE + 4	DAC 2 LSB Byte	BASE + 4
BASE + 5	DAC 2 MSB Byte	
BASE + 6	DAC 3 LSB Byte	BASE + 6
BASE + 7	DAC 3 MSB Byte	

BASE ADDRESS SELECTION

The ST-703 is a memory-mapped peripheral that occupies eight consecutive memory locations in the computer address space. The full 24-bit MULTIBUS addressing is supported, although the board may be used with CPU's that provide 16- or 20-bit addresses. The base address is selected by a combination of jumpers and DIP switches on the PC board. The board is factory-configured for 16-bit addressing and with a base address of 00FF10 hexidecimal.

24-, 20-, 16-BIT ADDRESS SELECT

Referring to the table below, remove or install the programming jumpers for the correct number of address select bits used in the system where the ST-703 is to be installed.

JUMPER	24 BIT	20 BIT	16 BIT
E103-E104	IN	OUT	OUT
E105-E106	IN	OUT	OUT
E107-E108	IN	OUT	OUT
E109-E110	IN	OUT	OUT
E111-E112	IN	IN	OUT
E 97-E 98	IN	IN	OUT
E 99-E100	IN	IN	OUT
E101-E102	IN	IN	OUT

BASE ADDRESS SELECTION

(1. Select a base address, in hexidecimal, and write it in Base Address, Hex.

(2. Convert the hexidecimal code to binary by writing 1's and 0's in the appropriate boxes (opposite Hex Bit Weighting).

(3. Set the base address desired on DIP switches S1 and S2. A closed switch (ON) corresponds to a 1 on the corresponding address line. An open (OFF) switch corresponds to a 0. Unused high order address switches must be left in the open (OFF) position. For example, if the CPU provides only 16 address lines, the address switches corresponding to ADR10 through ADR17 must be OFF.

1. To select a base address in hexidecimal use the following chart for changing configurations.

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DATEL®
INNOVATION and EXCELLENCE

ST-711/732
32 A/D, 2 D/A Analog Boards for MULTIBUS Microcomputers

SPECIAL FEATURES

- **Model ST-711 — 32 Single-Ended, 16 Differential Input A/D Channels**
- **Model ST-732 — 32 Single-Ended, 16 Differential Input A/D Channels plus 2 D/A Output Channels**

COMMON FEATURES

- **Operate with all MULTIBUS compatible microcomputers using 16-, 20-, or 24-bit addressing, 8-bit data transfer**
- **Work directly from RMX-86 Analog I/O Driver operating software**
- **Include a 10-stage jumper-selected, program-gatable pacer start clock, 1 mS to 1 second, crystal-controlled**
- **A/D input accept up to 16 user-installed shunts for 4-20 mA etc., current inputs**
- **FET-Input differential amplifiers accept on-board resistor for fixed high gain up to X1000 (10 mV full scale range)**
- **Include Programmable Gain Amplifier (X1, 2, 4, 8 gains)**
- **Work with the latest 80X86 and 680X0 CPU's**
- **May be used with any language or operating system**

GENERAL DESCRIPTION

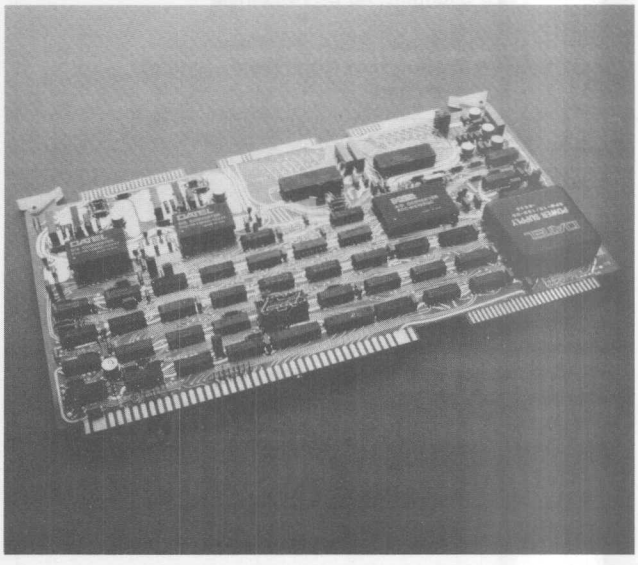
Functionally, DATEL's ST-711 and ST-732 are complete analog input systems for the MULTIBUS iSBC environment. These slide-in peripheral boards accept analog signals from up to 32 single-ended or 16 differential input channels, with the user able to reconfigure the boards using simple jumpers. In addition, the ST-732 provides two digital-to-analog output channels with current loop amplifiers

The differential input channels accept either voltage or current inputs. For current input applications, the user would install shunt resistors across each input channel into circuit pads provided .

Both boards have on-board ±15V power supplies, programmable gain amplifiers (PGA), and a 10-stage crystal pacer clock. Jumpers select the base memory address as well as control the conversion, scan, and external start interrupts.

Other important features include memory-mapped interfacing, addition of a FET input programmable differential amplifier, and complete pin-for-pin form, fit, and function identity to competitive iSBC-711/732 series A/D-D/A board systems. This last feature allows DATEL's ST-711/732 to operate directly from RMX-86 Analog I/O Drivers (Realtime Multitasking Executive Software).

For conversion control, the ST-711 includes on-board registers to store start and final A/D channel address, status bits, conversion modes and interrupt enables.



An A/D Converter auto-increment mode, which is program-selected, automatically advances the channel address after each conversion. Successive A/D samples will continue until the program-selected last channel address is reached.

The ST-732 is identical to the ST-711; both include two 12-bit hybrid DAC-HK D/A converters with input registers.

FUNCTIONAL DESCRIPTION

The A/D sections of the ST-711/732 use DATEL's hybrid technology ADC-HS combined successive approximation A/D converter and Sample/Hold Amplifier. The ADC-HS features 5 microseconds S/H acquisition time and 8 microseconds A/D conversion time and 12 bit binary resolution. System accuracy varies from ±0.05% of FSR ±1/2 LSB (10V range) to ±0.3% FSR ±1/2 LSB (10 mV range), including noise, quantization, nonlinearity, and dynamic errors.

The ST-711/732 employ DATEL's MX-1606 series fast CMOS multiplexers which incorporate ±35 Volts overvoltage protection. Input impedance is 100 meg-ohms minimum (power on) with 30 pA typical input bias current. Balanced inputs require 5 kilohms maximum source impedance to maintain accuracy and throughput rate.

All models inlcude an FET input differential amplifier which is wired as single-ended for the 32-channel models.

The standard A/D-D/A digital coding is offset binary (bipolar) but jumpers may easily be changed to straight binary (unipolar) or 2's complement (bipolar). Standard A/D-D/A analog signal ranges are ±10V full scale but may be jumper selected to ±5V, or +5V, or 10V unipolar.

SPECIFICATIONS

(Typical at 25 °C, dynamic conditions, unless noted).

GENERAL

Configurations available

Model ST-711
32S/16D A/D channels, no D/A channels

Model ST-732
32S/16D A/D channels, 2 D/A channels

Overall System Throughput (high level signals)
23,000 samples/second

ANALOG INPUTS

Number of Channels
32 single-ended or 16 differential
(Jumper-selected. 32S supplied standard)

Channel Expansion
May expand indefinitely by using additional ST-711/732 boards with different base address. Expansion limited by board slots and power.

Input Type
High impedance voltage input, non-isolated. Differential inputs are balanced.

Current Inputs
Up to 16 differential voltage inputs may be converted to differential current inputs with shunt resistors provided and installed by the user. Pads on the board will accommodate 4-20 mA, 1-5 mA, 10-50 mA and other ranges. 4-20 mA ranges require 250Ω, 1/4W ±1% resistors, ±100 ppm/ °C max.

Input Overvoltage
±35V sustained (no damage)

Input Capacitance to Ground
5 pF - Off channels, 100 pF - On channels

Full Scale Input Ranges
±10V, ±5V, ±2.5V, ±1.25V (supplied standard, selectable by 2-bit programmable gain code). Board pads are etched for the user to install a fixed gain resistor, providing down to ±10 mV full scale range.

Programmable Gain Amplifier
Supplied, X1, X2, X4, X8 gains (see ranges above). Fixed high gain X1000 optional (see above)

Input Impedance
100 mΩ minimum, differential or to ground (power on) 1.5 kΩ minimum (power off)

Input Source Resistance for Rated Specifications
5 K Ohms maximum (balanced)
1 K Ohms maximum (unbalanced)

Input Bias Current
30 pA typical, 200 pA maximum

Overall Accuracy at +25 °C
(Including 3-sigma noise and quantization error, dynamic response errors, referred to input, after initial calibration)

Gain	Accuracy
X1	±0.05% FSR ±1/2 LSB
X2	±0.07% FSR ±1/2 LSB
X4	±0.07% FSR ±1/2 LSB
X8	±0.07% FSR ±1/2 LSB
X100*	±0.1% FSR ±1/2 LSB
X1000*	±0.3% FSR ±1/2 LSB

*Requires rewiring diff. ampl. for fixed high gain

Common Mode Voltage Range
Within ±12V of analog common (signal plus common mode)

Common Mode Rejection
At Gain = 1

0 Hz	100 dB
100 Hz	80 dB
1 KHz	60 dB

At Gain = 8

0 Hz	120 dB
100 Hz	100 dB
1 KHz	80 dB

At Gain = 1000 (Requires rewiring dif. amp. for fixed high gain)

60 Hz	100 dB

Nonlinearity
±1/2 LSB

Differential Nonlinearity
±1/2 LSB

Resolution
12 binary bits (1 part in 4096)

Multiplexer Crosstalk from Off Channels
0.01% maximum

Sample/Hold Switch Feed Through
0.01% maximum

Sample/Hold Aperture Delay Time
100 nanoseconds, maximum

System Temperature Coefficients
Gain
±25 ppm of FSR/ °C (Gain X1)
±30 ppm of FSR/ °C (Gain X2, 4, 8)
Zero
±20 µV/ °C

A/D Conversion Period
20 microseconds

Amplifier Settling Time
(Input = ±FSR pk-pk step)
8 microseconds (HL)
110 microseconds (LL)

System Throughput Rate (High Level Inputs)
23,000 samples/seconds

A/D Digital Outputs
Offset binary (bipolar) - Supplied standard
Two's complement (bipolar)
Straight Binary (unipolar)

Output Data Format
12 bit binary group compatible to SBC-Series computers. The A/D Bit 1 (MSB) may be inverted by jumper to 2's complement coding.

ANALOG OUTPUTS (ST-732 only)

Number of Channels
2 non-isolated

Full Scale Output Voltage Ranges

0 to +5V	Jumpers may be rewired
0 to +10V	by the user or by DATEL
-5 to +5V	in OEM quantities
-10 to +10V	(Supplied Standard)

Digital Input coding

	Jumpers may be
Straight binary	rewired by the
2's Complement	user or by DATEL
	in OEM quantities
Offset Binary	(Supplied Standard)

Output Impedance
200 milliohms

Output Current
±5 mA, short circuit proof to ground

Slew Rate
10 V/µS (with no Ext. Cap. Load)

Settling Time
4 microseconds to within ±1/2 LSB of final value

Accuracy at +25 °C
±50 ppm of FSR/ °C

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CURRENT LOOP OUTPUTS
(Special Quantity order)

Full Scale Current Output Range
4 to 20 mA, unipolar. (May be rewired to other ranges by the user.)
Current Loop Load Resistance
0 to 500 Ohms
Current Loop Voltage Compliance
18 to 30V dc, unipolar, provided by the user
Accuracy at +25 °C
±50 ppm of FSR/ °C

PHYSICAL

Outline Dimensions
12W x 6.75D x 0.5H inches* (305 x 171 x 13 mm)
*Cards may be stacked adjacent if standard 0.60" spacing cages are used.
Pin-for-pin and card guide compatible to the Multibus SBC-Series computers
Weight
22 ounces (0.6 kg)
Operating Temperature Range
0 to +55 °C
Storage Temperature range
-25 to +85 °C
Relative Humidity
10% to 90%, non-condensing
Altitude
0 to 15,000 feet (4600 m)

MISCELLANEOUS

POWER CONSUMPTION
+5V dc ±5% @ 2.5 Amps. maximum
An on-board DC/DC Power Converter operated from +5V, is provided to supply regulated ±15V for linear circuits.
Programming and Architecture Type of Interface
Memory-mapped interface (I/O mapping available)
The ST-711/732 appears to the CPU as 16 consecutive memory locations with 4 unused locations
Compatibility
Pin-for-pin and card guide compatible to the Multibus, SBC-Series computers
Compatible Software
RMX-86 Analog I/O Drivers
Data Transfer - 8 bits only
The board does not make connection to BHEN/
Address Decode
16, 20, or 24 bits

Transfer Acknowledge Delay

The ST-711/732 responds with a Transfer Acknowledge (XACK) with any Read or Write Command. The XACK may be delayed to suit different processors. 16 delay steps are jumper-selected from 50 nanoseconds to 1.5 microseconds. Standard units are set to 50 nanoseconds.

Pacer Clock

Adjustable time-base consisting of a 10-stage binary divider capable of starting A/D conversions in the External Trigger Mode. Time-base periods are jumper-selected and the oscillator may be either crystal or RC controlled. The standard range is 97 microseconds to 1 second.

Interrupts

2 of 3 possible interrupts may be jumper-selected to one or both (INTA and INTB) interrupt lines. The interrupts are EOC (End of Conversion), EOS (End of Scan), and Pacer Clock. They are factory-jumpered as: INTA - EOS, INTB - EOC. Additionally, any of the 8 Multibus interrupts may be wired to any combination of the EOC, EOS Pacer Interrupts.

Memory Base Address

The 16-location starting base address is factory set at 00F700 (hex) but may be reassigned on 16-byte boundaries (LSB = 0) by altering a supplied DIP jumper plug.

Important: Be sure the host computer bus is 100% compatible to Multibus I

Ordering Guide

Model	Description
ST-711	32SE/16D A/D channels only
ST-732	32SE/16D A/D channels and 2 D/A channels

A user's manual is included.

Memory Address Assignments (All addresses in hex)

New Addr.	DATEL Supplied	Command	Function
Base + 0	00F700	Write	Load Command Register
Base + 0	00F700	Read	Read Status Register
Base + 1	00F701	Write	Load PGA and Ch. Addr. Register
Base + 1	00F701	Read	Read PGA and Ch. Addr. Register
Base + 2	00F702	Write	Load Last Chan. Addr. Register
Base + 3	00F703	Write	Clear Interrupts
Base + 4	00F704	Read	Read A/D Data LO Byte
Base + 5	00F705	Read	Read A/D Data HI Byte
Base + 8	00F708	Write	DAC 0 LO Byte to Hold Register
Base + 9	00F709	Write	DAC 0 HI Byte
Base + A	00F70A	Write	DAC 1 LO Byte to Hold Register
Base + B	00F70B	Write	DAC 1 HI Byte
Base + C to	00F70C/F &		Don't Use
Base + F	00F706/7		Don't Use

Acknowledge Interrupts (WRITE BASE +3)

Bits	Function
7,6	Not Used
5	0 = Clear EOC Interrupt
4	0 = Clear EOS Interrupt
3	0 = Clear Pacer Clock Interrupt
2,1,0	Not Used

Write to selected bit to acknowledge the interrupt. These bits do not disable interrupts.

A/D CONTROL ADDRESSES

Load Command Register (WRITE BASE + 0)

Bits	Function
7	Not Used
6	Not Used
5	1 = Enable End of Conversion (EOC) Interrupt
4	1 = Enable End of Scan (EOS) Interrupt
3	0 = Clear Board Busy Status
2	1 = Enable External Trigger, 0 = pgm start
1	1 = Enable Automatic Channel Address Increment 0 = Single Channel
0	1 = Enable A/D Conversion

Read Status Register (READ BASE + 0)

Bits	Function
7 (EOC)	1 = A/D Conversion Done, 0 = Data Invalid
6	1 = Scan Done
5	1 = EOC Interrupt Enabled
4	1 = EOS Interrupt Enabled
3	1 = Board is Busy
2	1 = External Trigger Enabled
1	1 = Auto-increment Enabled
0	1 = A/D Conversion Enabled

Read/Load PGA and Start Chan. Address Register (READ/WRITE BASE + 1)

Bits	Function	
7,6	00 = Gain X1 01 = Gain X2 10 = Gain X4 11 = Gain X8	The channel address auto sequences on the EOC rising edge if command 1=1
5	Not Used	
4	$1 = 2^4$	Start Chan. Addr. Select (1 of 32)
3	$1 = 2^3$	
2	$1 = 2^2$	
1	$1 = 2^1$	
0	$1 = 2^0$	

Load A/D Last Channel Address (WRITE BASE + 2)

Bits	Function	
7,6,5	Not Used	
4	$1 = 2^4$	Last Chan. Addr. Select (1 of 32)
3	$1 = 2^3$	
2	$1 = 2^2$	
1	$1 = 2^1$	
0	$1 = 2^0$	

All registers reset to zero at power up.

D/A COMMANDS

Load Hold Register with DAC LO Byte (WRITE BASE + 8 = DAC0, WRITE BASE + A = DAC1)

Bits	Function (Write this byte first)
7	DAC Bit 9
6	DAC Bit 10
5	DAC Bit 11
4	DAC Bit 12 (LSB)
3,2,1,0	Zeros

Load HI Byte to DAC; Load Hold Reg. to DAC (WRITE BASE + 9 = DAC0, WRITE BASE + B = DAC1) Enable DAC Input Register Strobe

Bits	Function* (Write this byte second)
7	DAC Bit 1 (MSB)
6	DAC Bit 2
5	DAC Bit 3
4	DAC Bit 4
3	DAC Bit 5
2	DAC Bit 6
1	DAC Bit 7
0	DAC Bit 8

*A/D-D/A convention is to label the converter's Most Significant Bit as Number 1 (MSB). (Note that D/A addressing is mapped adjacent to A/D addressing.)

A/D DATA ADDRESSES*

Read A/D Data HI Byte (READ BASE + 5)

Bits	Function (Read this byte second)
7	ADC Bit 1 (MSB)
6	ADC Bit 2
'	'
'	'
'	'
0	ADC Bit 8

Read A/D Data LO Byte (READ BASE + 4)

Bits	Function (Read this byte first)
7	ADC Bit 9
6	ADC Bit 10
5	ADC Bit 11
4	ADC Bit 12 (LSB)
3,2,1,0	Not Used, set to zeros

*Read B + 5 starts A/D conversion if command 0 = 1. Allow adequate settling time from channel address change until A/D start. Write 01h to BASE + 0 starts an A/D conversion by software.

The start channel is not reloaded at EOS. The channel address counter continues sequencing unless it is reloaded.

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INPUT RANGES

Programmable Gain	Unipolar		Bipolar		Low Level Unipolar	Low Level Bipolar
X1	0 to +5V	0 to +10V	±5V	±10V	Up to +80 mV	Up to ±1V
X2	0 to +2.5V	0 to +5V	±2.5V	±5V	Up to +40 mV	Up to ±500 mV
X4	0 to +1.25V	0 to +2.5V	±1.25V	±2.5V	Up to +20 mV	Up to ±200 mV
X8	0 to +675V	0 to +1.25V	±675V	±1.25V	Up to +10 mV	Up to ±100 mV

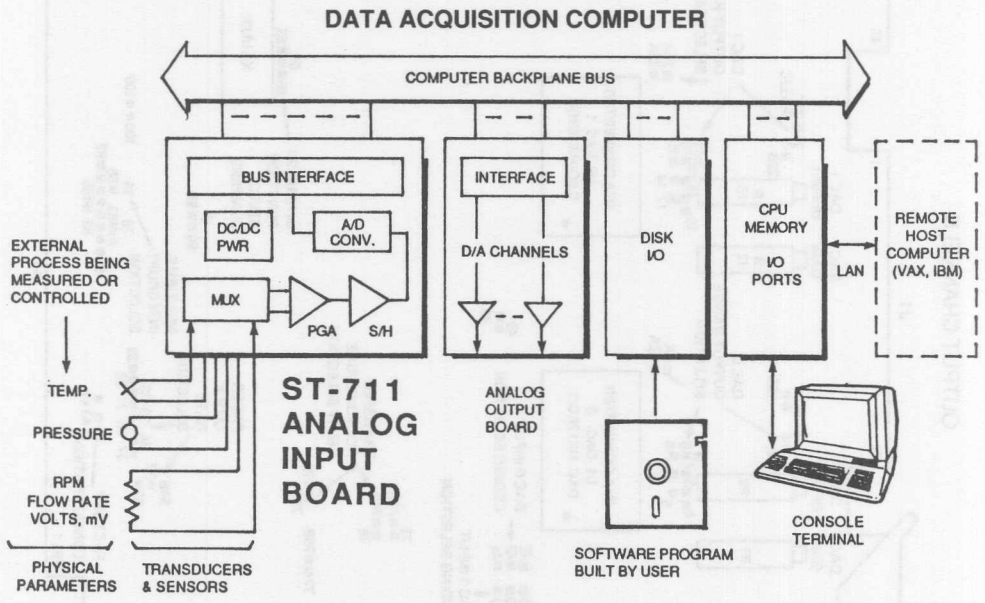
(Standard, Offset Binary)

Selected by on-board jumpers

Requires substitution by user of fixed gain resistor on the on-board differential amplifier.

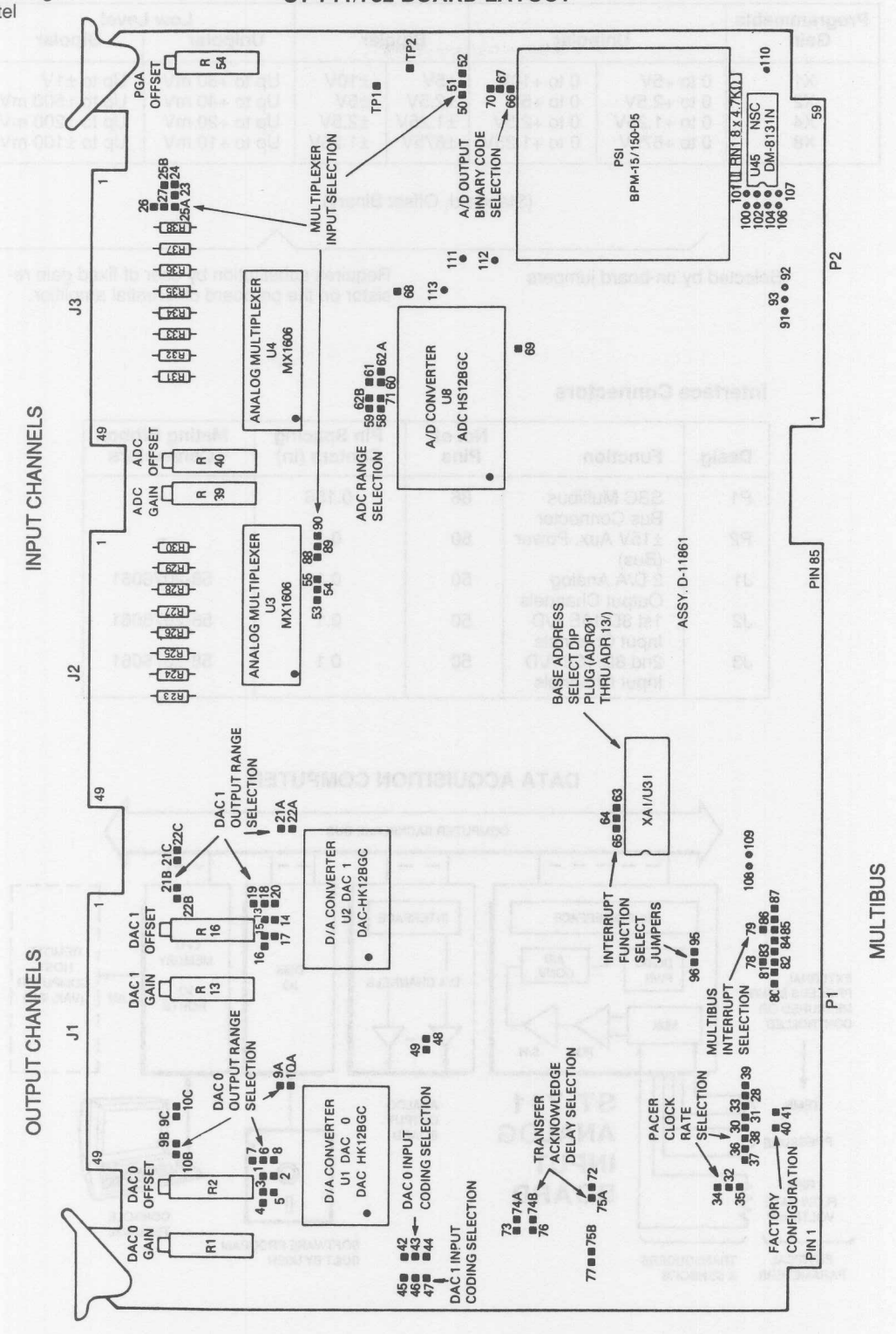
Interface Connectors

Desig.	Function	No. of Pins	Pin Spacing Centers (in)	Mating Ribbon Connectors
P1	SBC Multibus Bus Connector	86	0.156	–
P2	±15V Aux. Power (Bus)	60	0.1	–
J1	2 D/A Analog Output Channels	50	0.1	58-2076061
J2	1st 8D/16S A/D Input Channels	50	0.1	58-2076061
J3	2nd 8D/16S A/D Input Channels	50	0.1	58-2076061



Note: Pin numbering is reversed per Intel convention.

ST-711/732 BOARD LAYOUT



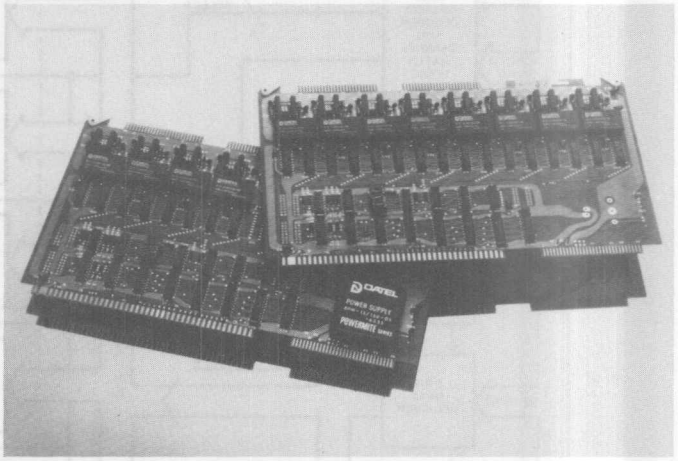
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ST-716
16-Bit D/A Board for MULTIBUS ISBC-80 Microcomputers

FEATURES

- 4 or 8 D/A channels, 16-bit resolution
- Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)
- Accurate to 0.005% of Full-Scale reading
- Complete hardware and software compatibility with MULTIBUS and ISBC-Series microcomputers
- 24-bit addressing
- Memory-mapped, with user-selectable base address
- Three user-selectable output ranges available: ±5 V dc, 0 to +10 V dc, and ±10 V dc
- Selectable Transfer Acknowledge delay (XACK/) ensures compatibility with different memory speeds



DATEL'S SineTrac ST-716 D/A BOARD PROVIDES END USERS AND OEM's WITH A MEANS OF PRODUCING HIGH RESOLUTION ANALOG OUTPUTS FROM THEIR MULTIBUS AND ISBC MICROCOMPUTERS, WITH 16 BITS OF RESOLUTION, THIS BOARD IS AN IDEAL CHOICE FOR PRECISION SERVO CONTROL AND SIMILAR APPLICATIONS.

GENERAL DESCRIPTION

The ST-716 provides 4 or 8 channels of digital-to-analog (D/A) conversion with 16 bits of resolution. Overall accuracy is within .005% of full scale reading. Voltage range outputs are jumper-selectable to ensure the board's compatibility with popular process control and test instrumentation.

Like other SineTrac products, the ST-716 is fully hardware and software compatible with its host ISBC or MULTIBUS computer. All necessary address decoders, logic controls, and data receivers are built in. The user simply slides the ST-716 into an Intel-compatible card cage and wires the analog outputs. The ST-716 is then ready as a memory-mapped D/A peripheral. It is addressed by the host computer as 16 consecutive memory locations with a user-defined base address. This memory-mapped format permits virtually unlimited D/A channel expansion by using multiple ST-716's, each with a different base address.

A systems manual is shipped with each board, providing installation instructions, theory of operation, and engineering drawings.

Figure 1 is a simplified block diagram of the ST-716, with the 8 D/A channel circuitry for Model ST-716D shown within dashed lines. The ST-716 is pin-compatible with DATEL's ST-724, ST-728, ISBC-724, and ISBC-728 analog output boards. The 4-channel ST-716's are software-compatible with the ST-724's and ST-728's while the 8-channel ST-716's are software-compatible with the ST-728's.

Data inputs to the ST-716 are from the host computer's bus. Input coding is offset binary.

Each channel uses a DATEL Model DAC-HP16B (or DAC-HP16B-1), a 16-bit hybrid device which offers linearity to ±0.003% of Full-Scale reading. The output of the converter is monotonic to 14 bits between +10°C and +40°C. Offset error on each channel has been adjusted to zero prior to shipping the boards. Trim pots on the board permit recalibration of zero (or offset) and range setting. The converter settles in 15μS to within ±0.005% of FSR. Zero tempco is ±5 ppm of FSR/°C, and gain tempco is within ±20 ppm of FSR/°C.

The board's base address is factory set at 0F710. However, the user may relocate the board's address anywhere up to FFFF0 by rewiring a 20-pin DIP plug supplied with the board. The user may also extend the addressing to a full 24 bits by soldering jumpers into holes provided on the board adding four more bits. This would extend the addressing capability to FFFFF0 hex.

In order to make the ST-716 compatible with different speed CPU and memory systems, a Transfer Acknowledge delay (XACK/Delay) circuit is provided. The user enables 16 jumper-selectable delays from .05 to 1.5 microseconds.

The ST-716 is fully bus, card cage, and software compatible with the MULTIBUS. The board is 12″W x 6.75″D x 0.5″H (305 x 172 x 13 mm). Multiple ST-716 boards can mount in adjacent card slots when used with a standard, .60″ spacing Intel card cage. The ST-716C and ST-716D draw all their power from the MULTIBUS +5V line.

An on-board dc-to-dc converter provides the ±15V to drive the board analog output circuits. The St-716 weighs approximately 11.2 ounces (0,318 kg). It can operate over a temperature range of 0 to +55°C with relative humidity from 10 to 90% (non-condensing), and from 0 to 15,000 feet (0 to 4600m) in altitude.

Refer to Figure 2 for information regarding the location of all user-selectable jumpers for addressing, XACK/Delay, and output range selection.

ORDERING INFORMATION
SEE LAST PAGE

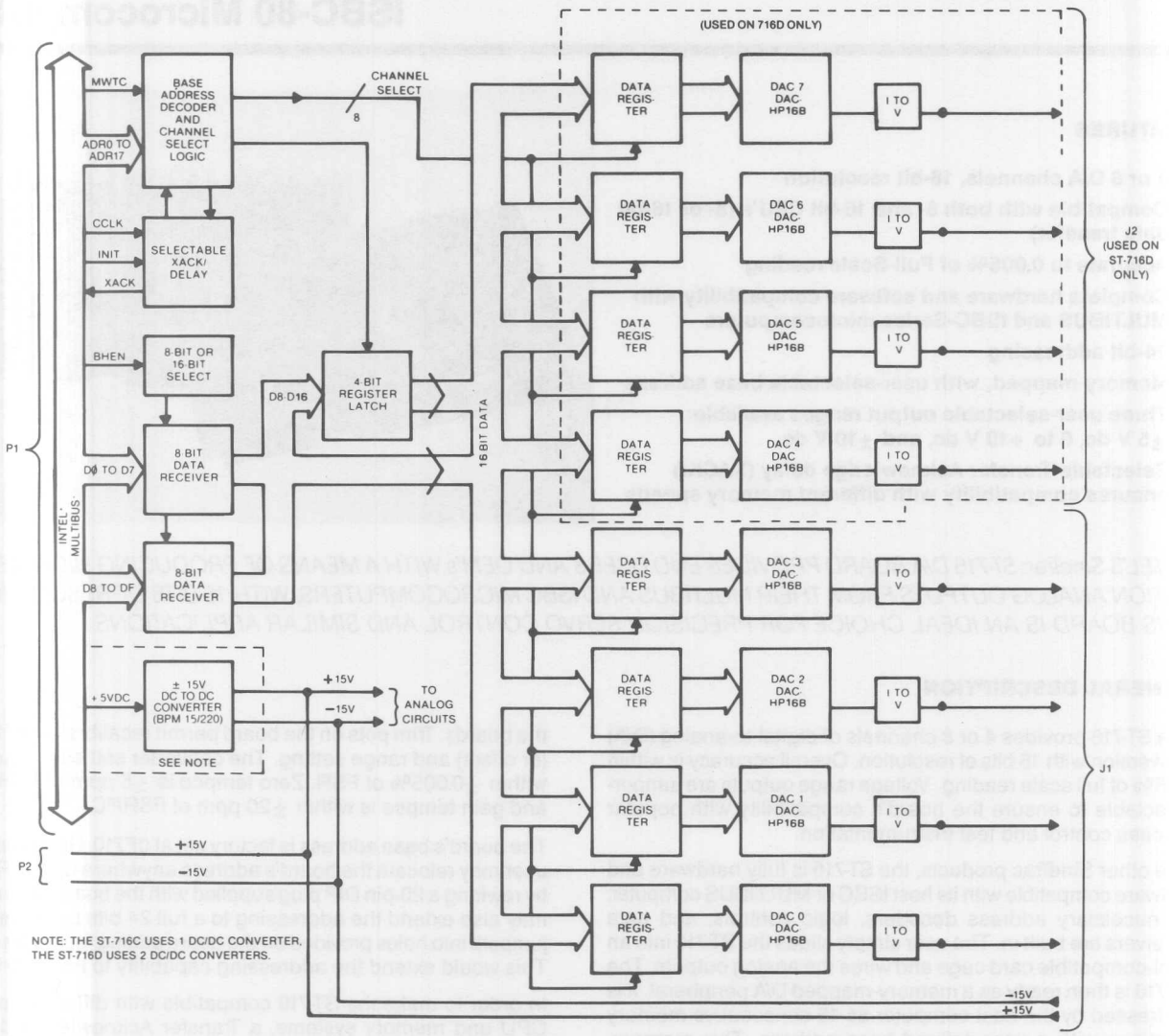


Figure 1. ST-716 Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, unless otherwise specified)

D/A ANALOG OUTPUT

Number of Channels
ST-716C . . . . . 4 D/A Channels with on-board dc-to-dc converter.
ST716D . . . . . 8 D/A channels with 2 on-board dc-to-dc converters.

Full Scale Output Ranges . . . . . ±5V, 0 to +10, ±10V dc
Digital Input Coding . . . . Offset Binary
Output Impedance . . . . . 50 Milliohms
Maximum Current Available on Voltage Outputs . . ±5 mA
Data Register Memory Mapping . . . . . Reserves a block of 16 consecutive memory locations

PERFORMANCE

Accuracy at +25°C . . . . . ±0.005% of FSR (includes noise and nonlinearity)
Settling Time . . . . . 10V change, 26 μSec. (to 0.005% FSR)
Power Supply Rejection . . ±0.002% FSR/%
Monotonicity . . . . . To 14 bits over +10°C to +40°C temp Range
Zero Temperature Drift (Unipolar Output Only) . . . Within ±5 ppm of FSR/°C
Offset Temperature Drift (Bipolar Output Only) . . ±8 ppm of FSR/°C
Gain Temperature Drift . . . Within ±20 ppm of FSR/°C

POWER CONSUMPTION

(From MULTIBUS +5 V dc, no load)

ST-716C . . . . . 2.0 Amps, typical
ST-716D . . . . . 4.2 Amps, typical

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FUNCTIONAL SPECIFICATIONS (cont.)

PHYSICAL

Outline Dimensions . . . . . 12.00″W x 6.75″D x 0.50″H (304,8 x 171,5 x 12,7 mm) ST-716 boards may be installed adjacent to each other in SBC card cages with 0.60″ spacing

Weight . . . . . 11.2 ounces (0,318 kg)

Operating Temperature Range . . . . . 0 to +55°C

Relative Humidity . . . . . 10% to 95%, non-condensing

Altitude . . . . . 0 to 10,000 ft.

SELECTION OF 8-BIT OR 16-BIT CPU's

The ST-716 board automatically changes to a 16-bit format when the BHEN/line on the MULTIBUS goes to zero volts (pin 27 of connector P1). A high input on BHEN/, consequently, sets the ST-716 for the 8-bit format.

DATA FORMAT

The ST-716 requires 16 bits of digital data, input from the host computer, for a single digital-to-analog (D/A) conversion. Table 1 indicates how 8-bit and 16-bit CPU's format this data.

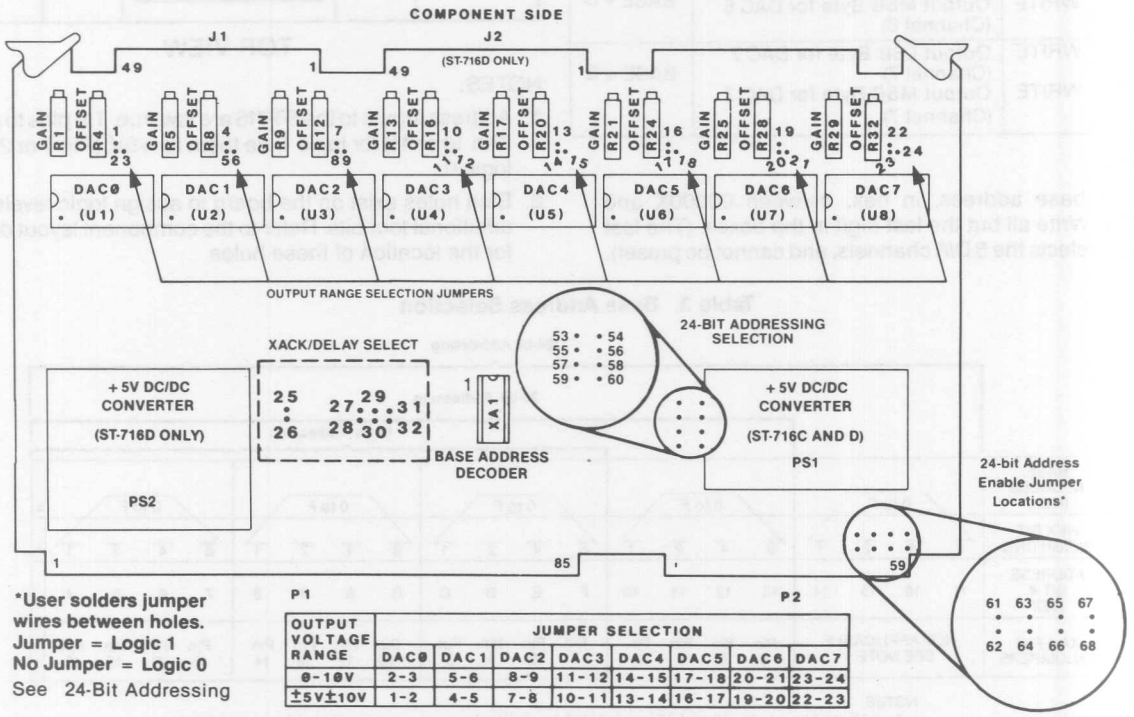
Note that 8-bit CPU's must transmit the 16 data bits in two bytes. The low byte contains the 8 least significant data bits; these are stored in a data register on the ST-716. The high byte contains the remaining 8 data bits. When the host transmits the high byte containing the 8 MSB's, the data register places the 8 LSB's also onto the selected DAC's input. Digital to-analog conversion then begins. Data transfer with a 16-bit CPU is somewhat simpler. All 16 data bits are transmitted as a single word. Data is loaded directly into the selected DAC, and a D/A conversion takes place.

Table 1. Data Formats for 8- or 16-Bit CPU's

SINGLE WORD, 16-BIT CPU	
HIGH BYTE (8-BIT CPU) BASE + 1,3,5,7,9,B,D, or F	LOW BYTE (8-BIT CPU) BASE + 0, 2,4,6,8,A,C, or E
D15 D14 D13 D12 D11 D10 D9 D8	D7 D6 D5 D4 D3 D2 D1 D0
DAC DATA 1 (MSB) DAC DATA 2 DAC DATA 3 DAC DATA 4 DAC DATA 5 DAC DATA 6 DAC DATA 7 DAC DATA 8	DAC DATA 9 DAC DATA 10 DAC DATA 11 DAC DATA 12 DAC DATA 13 DAC DATA 14 DAC DATA 15 DAC DATA 16 (LSB)

ST-716 REGISTER ASSIGNMENTS

Table 2 details the memory address assignments of the 16 memory locations the ST-716 occupies. Please note that when the ST-716 is used with 16-bit CPU's, every other (even-numbered) address location is used.



*User solders jumper wires between holes.
Jumper = Logic 1
No Jumper = Logic 0
See 24-Bit Addressing

OUTPUT VOLTAGE RANGE	JUMPER SELECTION							
	DAC0	DAC1	DAC2	DAC3	DAC4	DAC5	DAC6	DAC7
0-10V	2-3	5-6	8-9	11-12	14-15	17-18	20-21	23-24
±5V±10V	1-2	4-5	7-8	10-11	13-14	16-17	19-20	22-23

Figure 2. ST-716 Board Layout Drawing

BASE ADDRESS SELECTION

NOTE: The ST-716 may be used with both 8- and 16-bit microprocessors. Bits 10, 11, 12 and 13 are used or 20-bit addressing. Full 24-bit addressing would use these bits and address bits 14, 15, 16 and 17.

Use Table 3 as a worksheet to assign the base address.

Table 2. ST-716 Register Assignments

MEMORY ADDRESS (8-BIT CPU'S)	FUNC-TION	REGISTER ASSIGNMENT	MEMORY ADDRESS (16-BIT) CPU'S
BASE + 0	WRITE	Output LSB Byte for DAC 0 (Channel 0)	BASE + 0)
BASE + 1	WRITE	Output MSB Byte for DAC 0 (Channel 0)	
BASE + 2	WRITE	Output LSB Byte for DAC 1 (Channel 1)	BASE + 2
BASE + 3	WRITE	Output MSB Byte for DAC 1 (Channel 1)	
BASE + 4	WRITE	Output LSB Byte for DAC 2 (Channel 2)	BASE + 4
BASE + 5	WRITE	Output MSB Byte for DAC 2 (Channel 2)	
BASE + 6	WRITE	Output LSB Byte for DAC 3 (Channel 3)	BASE + 6
BASE + 7	WRITE	Output MSB Byte for DAC 3 (Channel 3)	
BASE + 8	WRITE	Output LSB Byte for DAC 4 (Channel 4)	BASE + 8
BASE + 9	WRITE	Output MSB Byte for DAC 4 (Channel 4)	
BASE + A	WRITE	Output LSB Byte for DAC 5 (Channel 5)	BASE + A
BASE + B	WRITE	Output MSB Byte for DAC 5 (Channel 5)	
BASE + C	WRITE	Output LSB Byte for DAC 6 (Channel 6)	BASE + C
BASE + D	WRITE	Output MSB Byte for DAC 6 (Channel 6)	
BASE + E	WRITE	Output LSB Byte for DAC 7 (Channel 7)	BASE + E
BASE + F	WRITE	Output MSB Byte for DAC 7 (Channel 7)	

Procedure

1. Select a base address, in hex, between 00000X and FFFFFX. Write all but the last digit in the boxes. (The last hex digit selects the 8 D/A channels, and cannot be preset).
2. Convert the hex code to binary by writing 1's and 0's in the boxes opposite "Hex Bit Weighting".
3. To set the ST-716 for a particular base address:

   Address bits 4 through 13: Connect the "1" pins together to pin 10 or 11 and the "0" pins together to pin 1 or 16, on DIP plug XA-1.
4. Address bits 0 through 3 select the 8 D/A channels and are not shown.
5. For 16-bit processors, bits 10, 11, 12 and 13 must be tied to pin 1.
6. XA-1 is a 20-pin DIP plug. (See Table 4)
7. Full 24-Bit addressing requires soldering jumper wires between etched holes provided on the ST-716 boards. See the ST-716 board component layout diagram for the location of these holes.

Table 4. Dip Plug XA-1 Pin Assignments

Set For Base Address of 0F700H

SIGNAL	PIN #		PIN #	SIGNAL
+5V	1		20	+5V
ADR 10	2		19	ADR 4
ADR C	3		18	ADR 5
ADR 11	4		17	ADR 6
ADR 12	5		16	ADR B
ADR 13	6		15	ADR 7
ADR F	7		14	ADR 8
ADR E	8		13	ADR 9
ADR D	9		12	ADR A
GND	10		11	GND

TOP VIEW

NOTES:

1. Address inputs to the ST-716 are low true. Tie pins to ground (Pin 10 or 11) for logic 1; tie them to +5V. (Pin 1 or 20) for a logic 0.
2. Etch holes exist on the board to assign logic levels to the additional four bits. Refer to the component layout diagram for the location of these holes.

Table 3. Base Address Selection

24-bit Addressing

20-bit Addressing

16-bit Addressing

BASE ADDRESS (HEX)	0 to F				0 to F				0 to F				0 to F				0 to F				X
HEX BIT WEIGHTING	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	•
ADDRESS BIT # HEX	17	16	15	14	13	12	11	10	F	E	D	C	B	A	9	8	7	6	5	4	
XA-1-PIN #'s/JUMPERS	NOT APPLICABLE SEE NOTE 1				Pin 6	Pin 5	Pin 4	Pin 2	Pin 7	Pin 8	Pin 9	Pin 3	Pin 16	Pin 12	Pin 13	Pin 14	Pin 15	Pin 17	Pin 18	Pin 19	

NOTES

1. Address bits 14, 15, 16 and 17 are enabled by placing jumpers across etched holes provided on the printed wiring board. See '24-Bit Addressing'
2. Boards are factory set for a base address of 00F10 hex.

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TRANSFER ACKNOWLEDGE (XACK/) DELAY SELECTION

The ST-716 board generates a Transfer Acknowledge (XACK/) signal in response to write commands from the host computer. It is sometimes desirable to delay this signal, in order to match the XACK/ signal to the host computer timing. The ST-716 has a jumper-selectable Transfer Acknowledge Delay (XACK/delay) ranging from 50 nanoseconds to 1.5 microseconds.

The accuracy of the XACK/delay is dependent in part on the duty cycle of the CCLK/signal generated by the computer, shorter duty cycles result in greater accuracy. The delay time is advanced on the leading edge of CCLK/; XACK/ is generated on the trailing edge of CCLK/.

Please refer to Table 5 for jumper configurations yielding different delay times.

Table 5. XACK/Delay Selection

DELAY µsec	JUMPERS			
*0.05	—	—	—	—
0.1	31-32	—	—	—
0.2	—	25-26	—	—
0.3	31-32	25-26	—	—
0.4	—	—	27-28	—
0.5	31-32	—	27-38	—
0.6	—	25-26	27-28	—
0.7	31-32	25-26	27-28	—
0.8	—	—	—	29-30
0.9	31-32	—	—	29-30
1.0	—	25-26	—	29-30
1.1	31-32	25-26	—	29-30
1.2	—	—	27-28	29-30
1.3	31-32	—	27-28	29-30
1.4	—	25-26	27-28	29-30
1.5	31-32	25-26	27-28	29-30

*Factory supplied configurations

OUTPUT RANGE CODING SELECTION

Datel ships the ST-716 boards with the full-scale output ranges configured as follows:

ST-716C1	± 5V dc
ST-716D1	0 to +10V dc
ST-716C2, D2	±10V dc

The particular jumper connections for individual DAC's appear in Table 6.

Tables 7 and 8 show the signals present on the output connectors of the ST-716.

Table 6. ST-716 Output Range Selection Jumpers

MODEL	RANGE	DAC 0	DAC 1	DAC 2	DAC 3	DAC 4	DAC 5	DAC 6	DAC 7
ST-716C2 ST-716D2	± 10V	1-2	4-5	7-8	10-11	13-14	16-17	19-20	22-23
ST-716C1	± 5V	1-2	4-5	7-8	10-11	13-14	16-17	19-20	22-23
ST-716D1	0 to + 10V	2-3	5-6	8-9	11-12	14-15	17-18	20-21	22-24

Table 7. J1 Analog Output Connections

WIRING SIDE	PIN #'S		COMPONENT SIDE
N/C	2	1	N/C
N/C	4	3	N/C
N/C	6	5	N/C
N/C	8	7	N/C
N/C	10	9	N/C
N/C	12	11	N/C
N/C	14	13	N/C
N/C	16	15	N/C
N/C	18	17	N/C
N/C	20	19	N/C
N/C	22	21	N/C
DAC 3, V OUT	24	23	DAC 3, ANA RTN
N/C	26	25	N/C
N/C	28	27	GND
DAC 2, V OUT	30	29	DAC 2, ANA RTN
N/C	32	31	N/C
N/C	34	33	GND
DAC 1, V OUT	36	35	DAC 1, ANA RTN
N/C	38	37	N/C
N/C	40	39	GND
DAC 0, V OUT	42	41	DAC 0, ANA RTN
N/C	44	43	N/C
N/C	46	45	GND
POWER COMMON	48	47	POWER COMMON
– 15V POWER[1]	50	49	+ 15V POWER[1]

NOTE: Pins 49 and 50 are outputs; 1 mA maximum (for reference only)

Table 8. J2 Analog Output Connections

WIRING SIDE	PIN #'S		COMPONENT SIDE
N/C	2	1	N/C
N/C	4	3	N/C
N/C	6	5	N/C
N/C	8	7	N/C
N/C	10	9	N/C
N/C	12	11	N/C
N/C	14	13	N/C
N/C	16	15	N/C
N/C	18	17	N/C
N/C	20	19	N/C
N/C	22	21	N/C
DAC 7, V OUT	24	23	DAC 7, ANA RTN
N/C	26	25	N/C
N/C	28	27	GND
DAC 6, V OUT	30	29	DAC 6, ANA RTN
N/C	32	31	N/C
N/C	34	33	GND
DAC 5, V OUT	36	35	DAC 5, ANA RTN
N/C	38	37	N/C
N/C	40	39	GND
DAC 4, V OUT	42	41	DAC 4, ANA RTN
N/C	44	43	N/C
N/C	46	45	GND
POWER COMMON	48	47	POWER COMMON
– 15V POWER[2]	50	49	+ 15V POWER[2]

NOTES:

1. J2 not used on 4 channel versions of ST-716.
2. Pins 49 and 50 are outputs; 1 mA maximum (for reference only)

24-BIT-ADDRESSING

For 16 or 20-bit addressing, Remove jumpers 53 through 68. For 24-bit addressing, install jumpers 61 to 62, 63 to 64, 65 to 66 and 67 to 68. Also install the following according to the desired address:

Address bit:	A17/	A16/	A15/	A14/
Jumper:	59-60	57-58	55-56	53-54

OPEN = "O", CLOSED = "1"

MSB Data Coding

Coding	Jumper
Straight or offset binary (non-inverted)	75 - 76
Two's complement bipolar (inverted MSB)	76 - 77

ORDERING INFORMATION

MODEL

ST-716 —
- 1 – ±5V dc, or 0 to +10V dc Output
- 2 – ±10V dc Output
- C-4 D/A Channels
- D-8 D/A Channels

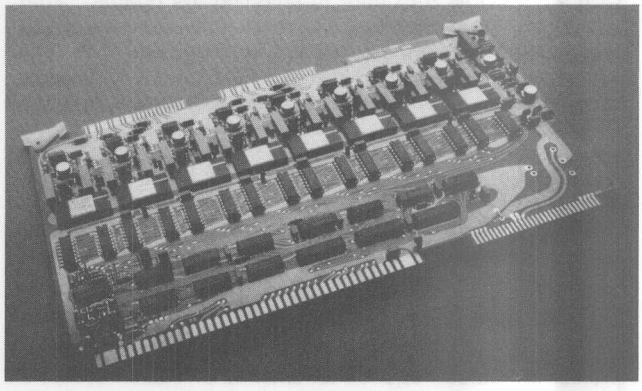
ACCESSORIES

Part Number	Description
31-20760040	Edge Connector for J1, J2, (Two supplied)

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DATEL®
INNOVATION and EXCELLENCE

ST-728
D/A Board for MULTIBUS Microcomputers



Compatible with: iSBC-80 Series
iSBC-86 Series

FEATURES

- **4 or 8 D/A channels, 12 bit resolution**
- **Compatible with both 8 and 16 bit CPU's (8 or 16 bit data transfer)**
- **16, 20-, or 24-Bit addressing**
- **Accurate to 0.05% of Full Scale Reading**
- **Complete hardware and software compatibility with MULTIBUS and iSBC-Series microcomputers**
- **Memory-mapped, with user selectable Base Address**
- **Three user-selectable input data codes: Straight Binary, Offset Binary, or Two's Complement**
- **Five user-selectable output ranges: ±5V dc, ±10V dc, 0 to +5V dc, 0 to +10V dc, and 4-20 mA current loop, individually selected for each channel**
- **Selectable Transfer Acknowledge Delay (XACK/) – ensures compatibility with different memory speeds**
- **ST-728A (4 D/A channels)**
  ST-728B (8 D/A channels)
  ST-728C (4 D/A channels, DC-to-DC **converter)**
  ST-728D (8 D/A channels, DC-to-DC **converter)**

APPLICATIONS

- **Computer control of analog input chart recorders, process receivers, proportional controllers, actuators and displays**
- **Custom automatic test equipment, computer simulators, modelling systems, pattern generators, multi-channel Waveform generators**

INTRODUCTION

DATEL expands its range of MULTIBUS and SBC compatible analog output boards with the SineTrac ST-728. The ST-728 provides 4 or 8 channels of digital to analog (D/A) conversion with 12 bits of resolution. Overall accuracy is within ±.05% of full scale reading. To ensure the board's compatibility with popular process receiver, control, and test instrumentation, four voltages ranges, and a 4-20 mA current loop output are jumper selectable for each D/A channel.

Like other SineTrac products, the ST-728 is fully hardware and software compatible with its host SBC or MULTIBUS computer. All necessary address decoders, logic controls, and data receivers are built in. The user simply slides the ST-728 into an Intel compatible card cage and wires the analog outputs. The ST-728 is then ready as a memory-mapped D/A peripheral. It is addressed by the host computer as 16 consecutive memory locations with a user-locatable base address. This memory-mapped format permits unlimited D/A channel expansion by using multiple ST-728's, each with a different base address.

The ST-728 is pin compatible with the ST-724 and SBC-724 analog output boards (4 channel ST-728's are software compatible with ST-724's; 8-channel ST-728's look like two ST-724's). Unlike the ST-724, however, the ST-728 may be used with both 8-and 16-bit microprocessors. The BHEN/ line on the MULTIBUS sets the ST-728's address decoders and data latches for compatibility with 8- or 16-bit computers.

A systems manual is shipped with each board, which provides a source listing of the Diagnostic as well as installation instructions, theory of operation, and engineering drawings.

GENERAL DESCRIPTION

Data inputs to the ST-728 are from the host computer's bus. Input coding may be straight binary, offset binary, or two's complement, and is selected by jumper plugs on the board.

The MULTIBUS BHEN/ line is used to set the ST-728's address and data decoding for compatibility with 8 to 16 bit CPU's. In the 8 bit mode, the twelve bits of data required for D/A conversion are acquired in two bytes. The lower byte contains the four lower data bits, and is loaded into a storage register for each D/A channel on the ST-728. The next data byte contains the 8 higher bits. Upon converion, the 8 MSB's and the 4 stored bits are loaded simultaneously into the DAC. In the 16-bit mode, all twelve data bits are transferred in a single byte.

Prior to being converted, the digital data is held in a storage register. Enabling the register loads the data into the digital to analog converter (DAC), and a conversion proceeds.

Each channel uses a 12-bit monolithic D/A device which of-

fers linearity to ±1/2 LSB of full scale reading. The output of the converter is monotonic, having a differential nonlinearity of ±1/2 LSB maximum. Offset error on each channel has been adjusted to zero prior to shipping the boards. Trim pots on the board permit recalibration of zero (or offset) and range settings using the supplied Diagnostic program. The converter settles in 400 nS to within 1/2 LSB of it final value. Zero tempco is ±2 ppm of FSR/°C, and gain tempco is within ±10 ppm of FSR/°C.

The output of each DAC is fed to its own I-to-V conversion amplifier. A total of 4 voltage output ranges may be jumper-selected by the user: ±5V and ±10V bipolar; and 0 to +5V or 0 to +10V single-ended. In addition, a V to I converter circuit is included for each D/A output channel. 4-20 mA output, usable with an output load from 0 to 500 Ω, is also jumper-selectable.

The current output requires an external excitation source – a +18V to + 30V dc regulated supply, capable of 25 mA per D/A channel, must be provided. Voltage and current output ranges on the ST-728 are selected independently for each channel, permitting a mix of different voltage or current outputs on a single board.

The ST-728 is a memory-mapped peripheral occupying 16 consecutive locations in the host computer's memory. The board's base address is factory set at 0F700[1]. However, the user may relocate his address anywhere up to FFFFFØH.

In order to make the ST-728 compatible with different speed CPU and memory systems, a Transfer Acknowledge Delay (XACK/Delay) circuit is provided. 16 delays from 0.05 to 1.5 µS are jumper-selectable by the user.

The ST-728 is fully bus, card cage, and software compatible with the MULTIBUS and with Intel RMX software. The board is 12.0"W x 6.75"D x 0.5"H (305 x 172 x 13 mm). Multiple ST-728 boards may be mounted in adjacent card slots when used with a standard, 0.60" spacing Intel card cage.

The ST-728C draws all its power from the MULTIBUS +5V line. An on-board DC-to-DC converter provides the ±15 to drive the board's analog output circuits. The ST-728A and ST-728B do not have a DC-to-DC converter. They are powered from the +5V MULTIBUS line, and an external ±15V supply.

The ST-728 weighs approximately 11.2 ounces (0,318 kg). It can operate over a temperature range of 0 to +55°C with relative humidity from 10 to 90% (non-condensing), and from 0 to 15,000 feet (0 to 4600 m) in altitude.

INPUT DATA FORMAT AND REGISTER ASSIGNMENTS

DATA FORMAT

The ST-728 requires 12 bits of digital data, input from the host computer for single digital to analog (D/A) conversion. The chart below indicates how 8-bit and 16-bit CPU's format this data.

SINGLE BYTE, 16-BIT CPU	
HIGH BYTE (8-bit CPU) BASE +1, 3, 5, 7, 9, B, D, or F	LOW BYTE (8-bit CPU) BASE +2, 4, 6, 8, A, C, or E
D15 D14 D13 D12 D11 D10 D9 D8	D7 D6 D5 D4 D3 D2 D1 D0

Note that 8-bit CPU's must transit the 12 data bits in two bytes. The low byte contains the four least significant data bits: these are stored in a data register on the ST-728. The high byte contains the remaining 8 data bits. When the high byte is transmitted, all twelve bits of data - the 4 LSB's stored in a register and the 8 MSB's coming from the host computer - are loaded into the input of the selected DAC on the ST-728, and D/A conversion proceeds. Data transfer with a 16-bit CPU is somewhat simpler. All twelve data bits are transmitted in a single word. Data is loaded directly into the selected DAC, and a D/A conversion takes place.

SELECTION OF 8-BIT OR 16-BIT CPU'S

The ST-728 board automatically changes to a 16-bit format when the BHEN/ line on the MULTIBUS goes to zero volts (pin 27 of the connector P1). A high input on BHEN/, consequently, sets the ST-728 for the 8-bit format.

ST-728 REGISTER ASSIGNMENTS

The following chart details the memory address assignments of the 16 memory locations the ST-728 occupies. Please note that when the ST-728 is used with 16-bit CPU's, every other (even-numbered) address location is used.

ST-728 REGISTER ASSIGNMENTS

MEMORY ADDRESS (8-bit CPU's)	FUNCTION	REGISTER ASSIGNMENT	MEMORY ADDRESS (16-bit CPU's)
BASE +0	WRITE	Output LSB Byte for DAC 0 (Channel 0)	BASE +0
BASE +1	WRITE	Output MSB Byte for DAC 0 (Channel 0)	
BASE +2	WRITE	Output LSB Byte for DAC 1 (Channel 1)	BASE +2
BASE +3	WRITE	Output MSB Byte for DAC 1 (Channel 1)	
BASE +4	WRITE	Output LSB Byte for DAC 2 (Channel 2)	BASE +4
BASE +5	WRITE	Output MSB Byte for DAC 2 (Channel 2)	
BASE +6	WRITE	Output LSB Byte for DAC 3 (Channel 3)	BASE +6
BASE +7	WRITE	Output MSB Byte for DAC 3 (Channel 3)	
BASE +8	WRITE	Output LSB Byte for DAC 4 (Channel 4)	BASE +8
BASE +9	WRITE	Output MSB Byte for DAC 4 (Channel 4)	
BASE +A	WRITE	Output LSB Byte for DAC 5 (Channel 5)	BASE +A
BASE +B	WRITE	Output MSB Byte for DAC 5 (Channel 5)	

Write the low byte first.

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FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, unless otherwise specified)

D/A ANALOG OUTPUT

Number of Channels

ST-728A, C - 4 D/A Channels
ST-728B, D - 8 D/A Channels
Indefinite channel expansion by separate, stand-alone ST-728 boards, each with a different base address; limited by available card slots, and power supply current.

Full Scale Output Ranges

±10V (standard) ±5V 0 to +10V 0 to +5V 4-20 mA	Jumper Selectable by User for each channel

Digital Input Coding

Straight Binary Offset Binary (Standard) 2's Complement	Jumper Selectable by User in 4-channel groups

Output Impedance
50 Milliohms
Maximum Current Available on Voltage Outputs
±5 mA @ ±10V short-circuit-proof to ground
Current Loop Load Resistance
0 to 500Ω
Current Loop External Excitation Voltage
+18V to +30V dc, regulated, user-supplied (25 mA/DAC, max.)

ADDRESSING

Reserves a block of 16 consecutive memory locations. Base address may be located by jumper selection anywhere in the host computer's memory on 16-byte boundaries.

PERFORMANCE

Accuracy at +25°C
±0.05% of FSR (includes noise and nonlinearity)
Linearity Error, max. ±1/2 LSB
Linearity Error, 0°C to +70°C ±1 LSB
Differential Linearity Error ±1/2 LSB
Monotonicity
Monotonic over 0 to +55 °C temp. range
Zero Temperature Drift
(Unipolar Output only) Within ±2 ppm of FSR/°C
Offset Temperature Drift
(Bipolar Output only) Within ±5 ppm of FSR/°C

Gain Temperature Drift
Within ±10 ppm of FSR/°C
Settling Time (Board)
5 µS to within 1/2 LSB of final value

PHYSICAL

Outline Dimensions
12.00"W x 6.75"D x 0.50"H (304,8 x 171,5 x 12,7 mm)
ST-728 boards may be installed adjacent to each other in SBC card cages with 0.60" spacing
Weight (ST-728B) 11.2 ounces (0,318 kg)
Operating Temperature Range 0 to + 55°C
Relative Humidity 10% to 95%, non-condensing
Altitude 0 to 15,000 ft

POWER CONSUMPTION

All ST-728 models use some +5V power from the MULTIBUS. The ST-728C (4 channels) has an on-board DC-DC converter, so that *all* board power comes from the +5V line on the MULTIBUS. The ST-728A (4 channels no DC-to-DC) and ST-728B (8 channels, no DC-to-DC) require external ±15V supplies, input to the board via connector P2. The chart below summarizes the ST-728 board power requirements.

	from +5V MULTIBUS	+15V (P2)	-15V (P2)
ST-728A	750 mA	140 mA (150 mA)	70 mA (90 mA)
ST-728B	1000 mA	110 mA (130 mA)	275 mA (300 mA)
ST-728C	1500 mA max.	N/A	N/A
ST-728D	2500 mA max.	N/A	N/A

Except as noted, current readings are:
typical, (with output load)
typical, without output load

GENERAL

Bus Compatibility
Pin-for-pin, card guide, and program compatible with MULTIBUS and SBC-series microcomputers.

CPU Compatibility
May be used with either 8-bit or 16-bit microprocessors.

Connectors

PCB edgeboard, 0.062 inch thick board, 50 pins, dual row (2 x 25) on 0.100 inch centers, P/N 2076040. Two supplied.

ANALOG OUTPUT CONNECTIONS

J1 (DAC'S 0, 1, 2, 3)

WIRING SIDE	PIN #'S		COMPONENT SIDE
NO CONNECTION	2	1	NO CONNECTION
NO CONNECTION	4	3	NO CONNECTION
NO CONNECTION	6	5	NO CONNECTION
NO CONNECTION	8	7	DAC 3, REF RTN
NO CONNECTION	10	9	DAC 3, EXT REF
NO CONNECTION	12	11	DAC 2, REF RTN
NO CONNECTION	14	13	DAC 2, EXT REF
NO CONNECTION	16	15	DAC 1, REF RTN
NO CONNECTION	18	17	DAC 1, EXT REF
NO CONNECTION	20	19	DAC 0, REF RTN
NO CONNECTION	22	21	DAC 0, EXT REF
DAC 3, V OUT	24	23	DAC 3, ANA RTN
DAC 3, I RTN	26	25	DAC 3, I RTN
DAC 3, LOOP V+	28	27	GND
DAC 2, V OUT	30	29	DAC 2, ANA RTN
DAC 2, I OUT	32	31	DAC 2, I RTN
DAC 2, LOOP V+	34	33	GND
DAC 1, V OUT	36	35	DAC 1, ANA RTN
DAC 1, I OUT	38	37	DAC 1, I RTN
DAC 1, LOOP V+	40	39	GND
DAC 0, V OUT	42	41	DAC 0, ANA RTN
DAC 0, I OUT	44	43	DAC 0, I RTN
DAC 0, LOOP V+	46	45	GND
POWER COMMON	48	47	POWER COMMON
-15V POWER[1]	50	49	+15V POWER[1]

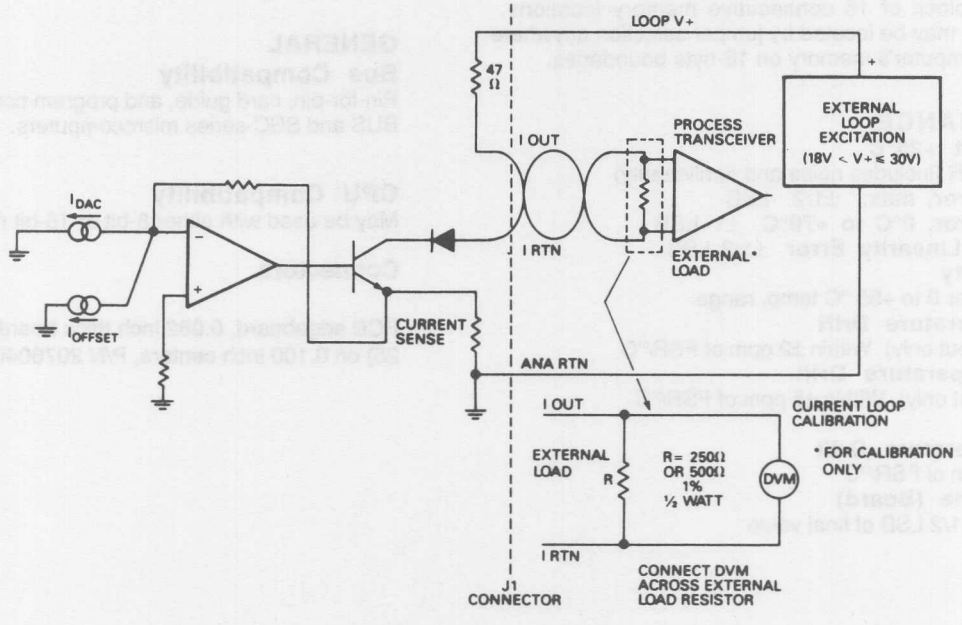
NOTE: 1. 49 & 50 are outputs; 1 mA max (for ref. only).

J2 (DAC'S 4, 5, 6, 7)[1]

WIRING SIDE	PIN #'S		COMPONENT SIDE
NO CONNECTION	2	1	NO CONNECTION
NO CONNECTION	4	3	NO CONNECTION
NO CONNECTION	6	5	NO CONNECTION
NO CONNECTION	8	7	DAC 7, REF RTN
NO CONNECTION	10	9	DAC 7, EXT REF
NO CONNECTION	12	11	DAC 6, REF RTN
NO CONNECTION	14	13	DAC 6, EXT REF
NO CONNECTION	16	15	DAC 5, REF RTN
NO CONNECTION	18	17	DAC 5, EXT REF
NO CONNECTION	20	19	DAC 4, REF RTN
NO CONNECTION	22	21	DAC 4, EXT REF
DAC 7, V OUT	24	23	DAC 7, ANA RTN
DAC 7, I OUT	26	25	DAC 7, I RTN
DAC 7, LOOP V+	28	27	GND
DAC 6, V OUT	30	29	DAC 6, ANA RTN
DAC 6, I OUT	32	31	DAC 6, I RTN
DAC 6, LOOP V+	34	33	GND
DAC 5, V OUT	36	35	DAC 5, ANA RTN
DAC 5, I OUT	38	37	DAC 5, I RTN
DAC 5, LOOP V+	40	39	GND
DAC 4, V OUT	42	41	DAC 4, ANA RTN
DAC 4, I OUT	44	43	DAC 4, I RTN
DAC 4, LOOP V+	46	45	GND
POWER COMMON	48	47	POWER COMMON
-15V POWER [2]	50	49	+15V POWER [2]

NOTES: 1. J2 not used on 4 channel versions of ST-728
2. 49 & 50 are outputs; 1 mA max (for ref. only).

ST-728



Typical ST-728 Current Loop Wiring

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D/A CALIBRATION PROCEDURE (Performed with optional Diagnostic Program)

Calibration of the ST-728 should be performed every 90 days or whenever the Analog Output Range jumpers are reconfigured. More frequent calibration may be indicated in adverse operating conditions. The Diagnostic program listed in the ST-728 user manual was written as part of the calibration procedure. Please see the section entitled "Diagnostic Program".

1. Set the board jumpers for the desired output range: 0 to +5V, 0 to +10V, 4-20 mA, ±5V, or ±10V. See "Output Range Selection" for details.
2. Connect a digital voltmeter (Fluke 8800A or equivalent) to the outputs of Channel 0 (DAC 0). For voltage ranges, measure between "V OUT" and "ANA RTN". For current ranges the user must supply a precision 25Ω or 500Ω resistor; voltage measurements are then made across this resistor (see Note 1, bottom of Calibration Table.)
3. Using the Diagnostic program, select the "Calibration Test", Call Key "C".
4. The teletypewriter will respond by printing out:
   CALIBRATION TEST
   CHANNEL-
5. Enter character "0" to select Channel 0 (DAC 0)
   CHANNEL-0
   HEX DATA
6. Making reference to the Calibration Table, enter the hex code for the –Full Scale output voltage(or current), then enter a Carriage Return. Adjust the OFFSET potentiometer, until the reading on the DVM corresponds to the –Full Scale reading from the table.
7. Refer again to the Calibration Table, and enter the hex code for +Full Scale voltage or current. Adjust the GAIN potentiometer until the reading on the DVM is the +Full Scale voltage as indicated in the table.
8. Repeat steps 6 and 7.
9. Calibration for Channels 1 through 7 (DACs 1 through 7) is the same as for Channel 0.
10. The complete calibration may now be checked using the Calibration Table. Any hex value on the table may be entered followed by a carriage return. The corresponding analog output should appear on the DVM.

CALIBRATION TABLE

ANALOG OUTPUT						4-DIGIT HEX INPUT	
UNIPOLAR (STRAIGHT BINARY)				BIPOLAR (OFFSET OR 2'S COMPLEMENT)		STRAIGHT OR OFFSET BINARY- NO SIGN EXTENSION	2'S COMPLEMENT WITH SIGN EXTENSION
VOLTAGE		4-20mA CURRENT[1]					
0 TO +5V	0 TO +10V	500Ω LOAD LOOP V+>18V	200Ω LOAD LOOP V+>15V	±5V	±10V		
4.9988V	9.9976V	9.9980V	4.9990V	4.9976V	9.9951V	FFF0	7FF0
4.9976V	9.9951V	9.9961V	4.9980V	4.9951V	9.9902V	FFE0	7FE0
4.9951V	9.9902V	9.9922V	4.9961V	4.9902V	9.9805V	FFC0	7FC0
4.9902V	9.9805V	9.9844V	4.9922V	4.9805V	9.9609V	FF80	7F80
4.9805V	9.9609V	9.9687V	4.9844V	4.9609V	9.9219V	FF00	7F00
4.9609V	9.9219V	9,9375V	4.9687V	4.9219V	9.8437V	FE00	7E00
4.9219V	9.8437V	9.8750V	4.9375V	4.8437V	9.6875V	FC00	7C00
4.8437V	9.6875V	9.7500V	4.8750V	4.6875V	9.3750V	F800	7800
4.6875V	9.3750V	9.5000V	4.7500V	4.3750V	8.7500V	F000	7000
4.3750V	8.7500V	9.0000V	4.5000V	3.7500V	7.5000V	E000	6000
3.7500V	7.5000V	8.0000V	4.0000V	2.5000V	5.0000V	C000	4000
2.5000V	5.0000V	6.0000V	3.0000V	0.0000V	0.0000V	8000	0000
1.2500V	2.5000V	4.0000V	2.0000V	-2.5000V	-5.0000V	4000	C000
0.6250V	1.2500V	3.0000V	1.5000V	-3.7500V	-7.5000V	2000	A000
0.3125V	0.6250V	2.5000V	1.2500V	-4.3750V	-8.7500V	1000	9000
0.1563V	0.3125V	2.2500V	1.1250V	-4.6875V	-9.3750V	0800	8800
0.0781V	0.1563V	2.1250V	1.0625V	-4.8437V	-9.6875V	0400	8400
0.0391V	0.0781V	2.0625V	1.0312V	-4.9219V	-9.8437V	0200	8200
0.0196V	0.0391V	2.0312V	1.0156V	-4.9609V	-9.9219V	0100	8100
0.0098V	0.0196V	2.0156V	1.0078V	-4.9805V	-9.9609V	0080	8080
0.0049V	0.0098V	2.0078V	1.0039V	-4.9902V	-9.9805V	0040	8040
0.0024V	0.0049V	2.0039V	1.0020V	-4.9951V	-9.9902V	0020	8020
0.0012V	0.0024V	2.0020V	1.0010V	-4.9976V	-9.9951V	0010	8010
0.0000V	0.0000V	2.0000V	1.0000V	-5.0000V	-10.0000V	0000	8000

Note 1: Both the 250Ω and the 500Ω resistors (0.1% precision) provide 4 to 20 mA output. The current output circuit is calibrated in terms of voltage since most digital multimeters provide greater resolution and accuracy on voltage measurements than on current.

The voltages listed are those measured across a 250Ω or a 500Ω precision resistor, connected between "I RTN" and "I OUT" on any DAC output. A user-supplied DC regulated voltage, V+ (+15V < V+ ≤ +30V for 250Ω resistor, +18V < V+ ≤ +30V for 500Ω resistor; 25 mA max) is required for current output and calibration, and should be connected to "V+ LOOP". The supply providing V+ should be grounded at "ANA RTN".

TRANSFER ACKNOWLEDGE (XACK/) DELAY SELECTION

The ST-728 board generates a Transfer Acknowledge (XACK) signal in response to Write commands from the host computer. It is sometimes desirable to delay this signal in order to match the XACK/ signal to the host computer timing. A jumper selectable Transfer Acknowledge Delay (XACK/delay) ranging from 50 nanoseconds to 1.5 microseconds is available in the ST-728.

The accuracy of the XACK/delay is dependent in part on the duty cycle of the CCLK/ signal generated by the computer-shorter duty cycles result in greater accuracy. The delay time is advanced on the leading edge of CCLK/; XACK/ is generated on the trailing edge of CCLK/.

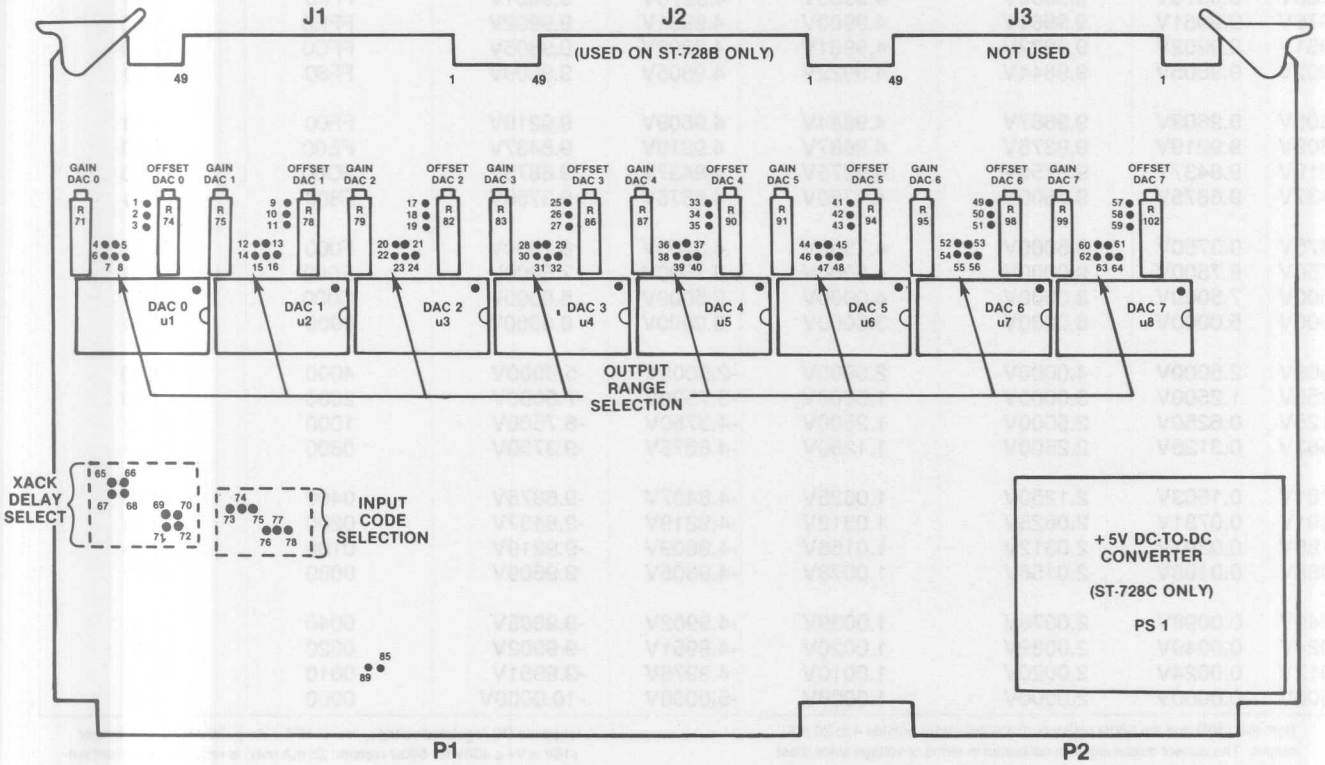
Please refer to the table for jumper configurations yielding different delay times.

XACK/ DELAY SELECTION

DELAY µsec.	JUMPERS			
0.05*	–	–	–	–
0.1	67-68	–	–	–
0.2	–	65-66	–	–
0.3	67-68	65-66	–	–
0.4	–	–	69-70	–
0.5	67-68	–	69-70	–
0.6	–	65-66	69-70	–
0.7	67-68	65-66	69-70	–
0.8	–	–	–	71-72
0.9	67-68	–	–	71-72
1.0	–	65-66	–	71-72
1.1	67-68	65-66	–	71-72
1.2	–	–	69-70	71-72
1.3	67-68	–	69-70	71-72
1.4	–	65-66	69-70	71-72
1.5	67-68	65-66	69-70	71-72

*Factory supplied configuration

COMPONENT SIDE



ST-728 Board Layout

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BASE ADDRESS SELECTION

(For Assembly D–11625, Revision F or later)

Base Address (Hexadecimal)	[see note 2] (Ø to F)	(Ø to F)	(Ø to F)	(Ø to F)	(Ø to F)	* (Ø)
Hex bit weighing	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	
Address Bit (Hex)	17 16 15 14	13 12 11 10	F E D C	B A 9 8	7 6 5 4	3 - 0
Jumper (see note 1)	A A A A 17 16 15 14	A A A A 13 12 11 10	AF AE AD AC	AB AA A9 A8	A7 A6 A5 A4	

Note 1: Jumper Out =" Ø", Jumper In = "1".
* Address bits 3 - Ø are decoded by D/A channel addressing.

Note 2: For 24-bit addressing, install jumper 80-81. For 16- or 20-bit addressing, remove jumper 80-81.

Note 3: To control 8- or 16-bit transfers by detecting BHEN/, remove jumper 84-85. Install jumper 84-85 to ground BHEN/ (always low).

OUTPUT RANGE INPUT CODING SELECTION

The ST-728's D/A output channels may be set independently for any of four voltage ranges or a single current output range. Full scale ranges of ±10V, ±5V, 0 to +10V, 0 to +5V, or 4–20 mA may be jumper-selected according to the chart below. Input digital coding may be offset binary, 2's complement, or straight binary. Again, refer to the chart below for details.

The ST-728 board is normally shipped with jumpers set for the ±10V output, and an offset binary input coding. Please note that whenever there is a change in output range on a given channel, that channel should be recalibrated.

INPUT CODE SELECTION JUMPERS

CODE	DAC 0 TO DAC 3	DAC 4 TO DAC 7
Unipolar or Offset Bin. (Standard)	74-75	77-78
2's Complement	73-74	76-77

OUTPUT RANGE SELECTION JUMPER

RANGE	DAC 0	DAC 1	DAC 2	DAC 3	DAC 4	DAC 5	DAC 6	DAC 7
±10V (Standard)	2-3 4-5	10-11 12-13	18-19 20-21	26-27 28-29	34-35 36-37	42-43 44-45	50-51 52-53	58-59 60-61
±5V	2-3 4-6	10-11 12-14	18-19 20-22	26-27 28-30	34-35 36-38	42-43 44-46	50-51 52-54	58-59 60-62
0 to +10V	4-6	12-14	20-22	28-30	36-38	44-46	52-54	60-62
0 to +5V	4-6 5-7	12-14 13-15	20-22 21-23	28-30 29-31	36-38 37-39	44-46 45-47	52-54 53-55	60-62 61-63
4 to 20 mA Current Loop	1-2 7-8	9-10 15-16	17-18 23-24	25-26 31-32	33-34 39-40	41-42 47-48	49-50 55-56	57-58 63-64

ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
ST-728A2/24	4 D/A Channels, no DC-DC Converter (±15V dc, +5V dc power required)
ST-728B2/24	8 D/A Channels, no DC-DC Converter (±15V dc, +5V dc power required)
ST-728C2/24	4 D/A Channels, with DC-DC Converter (+5V dc power required)
ST-728D2/24	8 D/A Channels, with DC-DC Converter (+5V dc power required)
UM-ST-728	ST-728 Manual (Spare; one supplied with board)

Standard (2/24) versions include the current loop option. Versions without current loops(1/24) are available for scheduled, quantity orders.

Contact **DATEL** for:

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AN-1 High-Speed AD Converter Designs: Layout and Interfacing Pitfalls
AN-2 Picking the Right S/H Amp for Various Data Acquisition Needs
AN-3 Data Converters: Getting to Know Dynamic Specs
AN-4 Understanding Data Converters' Frequency Domain Specifications
AN-5 Subranging ADC's, Architectures, Specifications & Testing
AN-6 Seeing is Believing: A/D Converters Make the Difference in Imaging Applications
AN-7 Modifying Start Convert Pulses Using Commercially Available Devices
AN-8 Heat Sinks for DIP Data Converters
AN-9 Performance Considerations for High-End PC A/D Boards

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Placing an Order

Placing an Order

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